ASSIGNMENT 4

Name: - Khelan Vaishnav

ID NO.: - 21EL038

Division: - 04

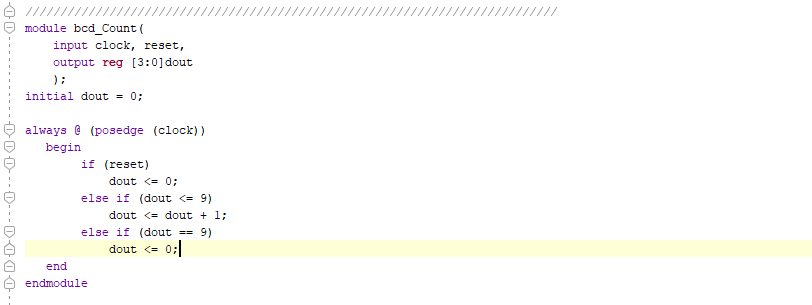
Year: - 2023-24

Subject: - Digital System Design (3EL42)

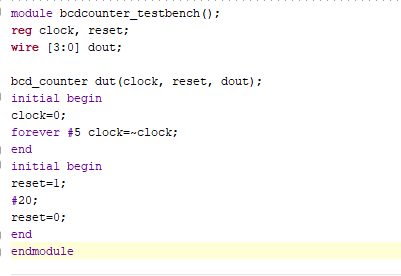
Branch: - Electronics (EL)

Q1. BCD TIMECOUNT

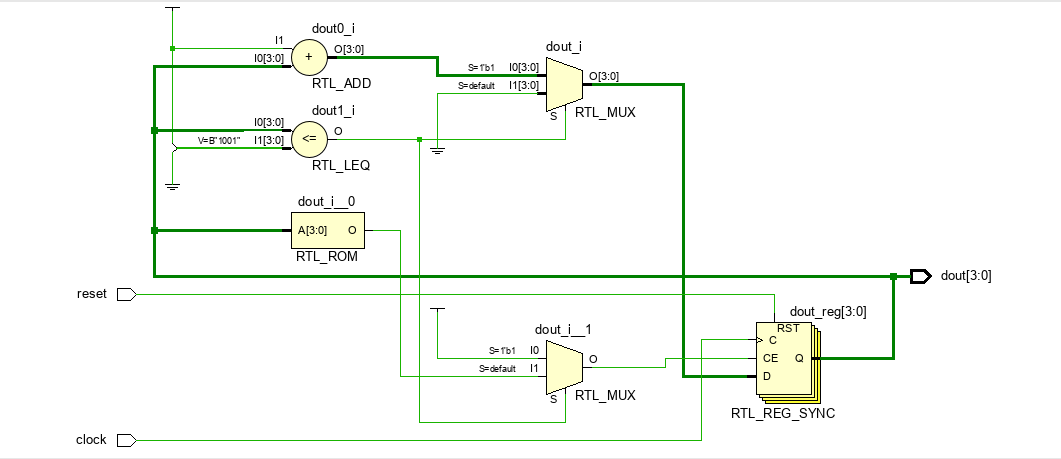
VERILOG CODE:-



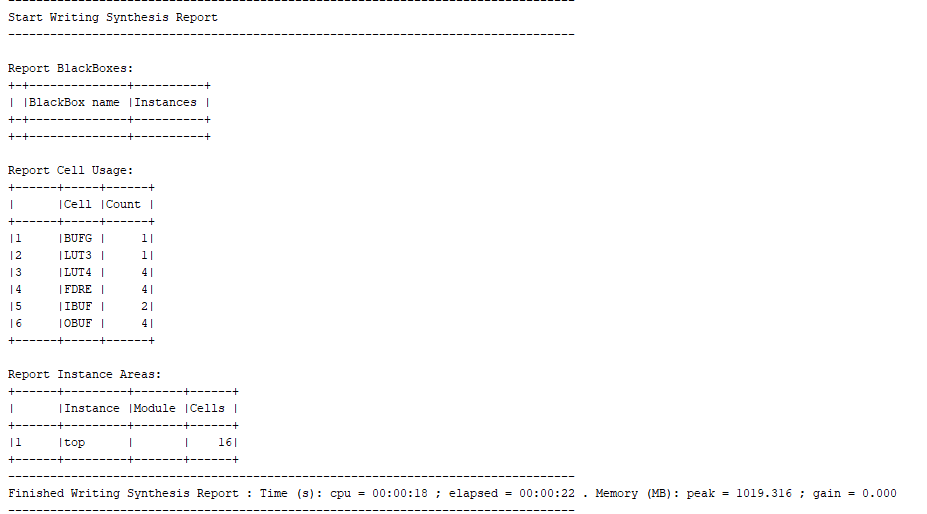
TEST BENCH:-



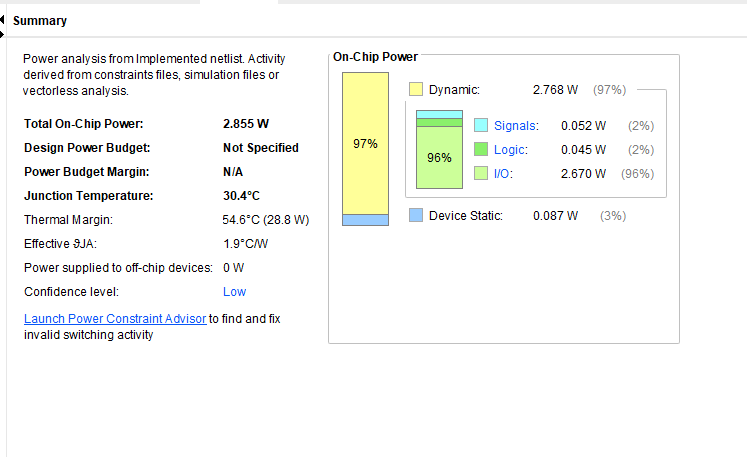
RTL SCHEMATIC:-



SYNTHESIS REPORT:-



POWER REPORT:-

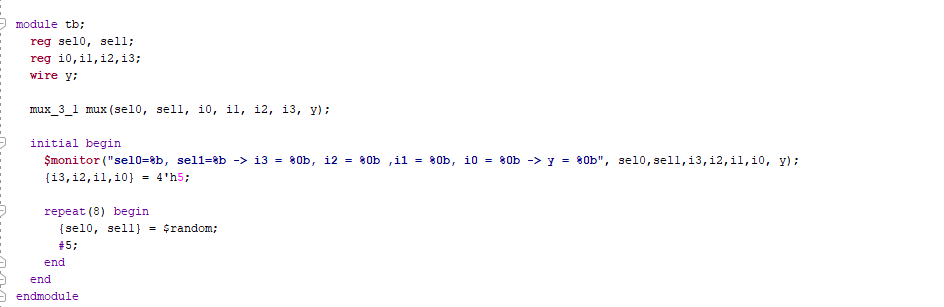


Q2. 3-1 MUX

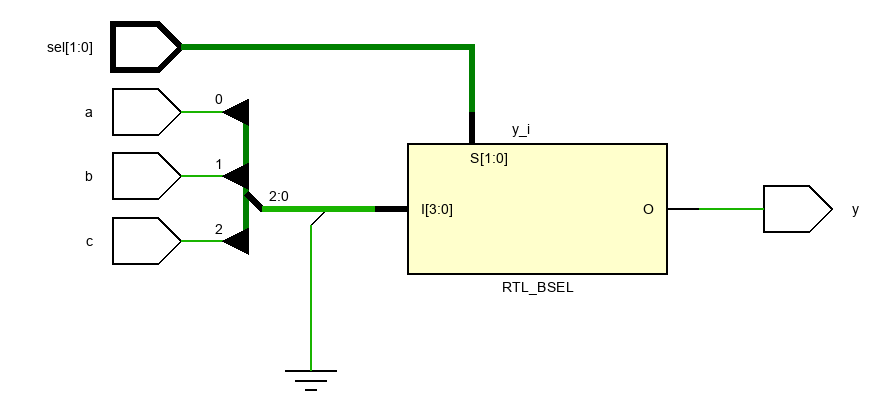
VERILOG CODE:-



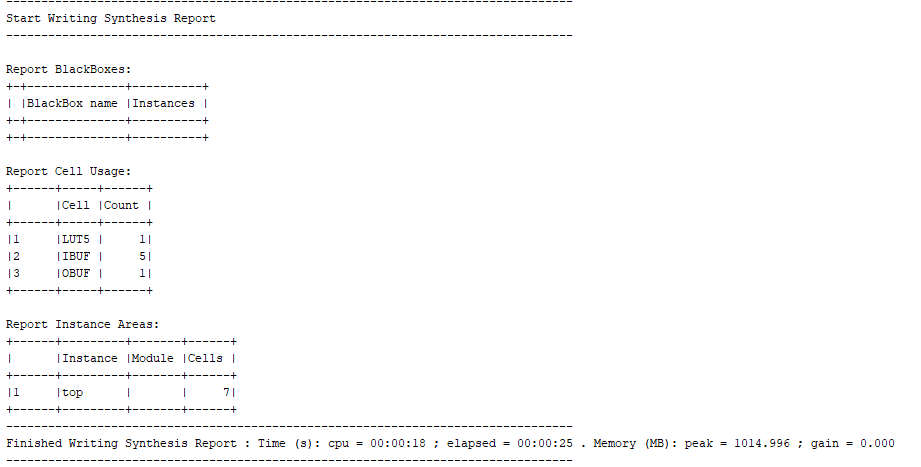
TESTBENCH:-



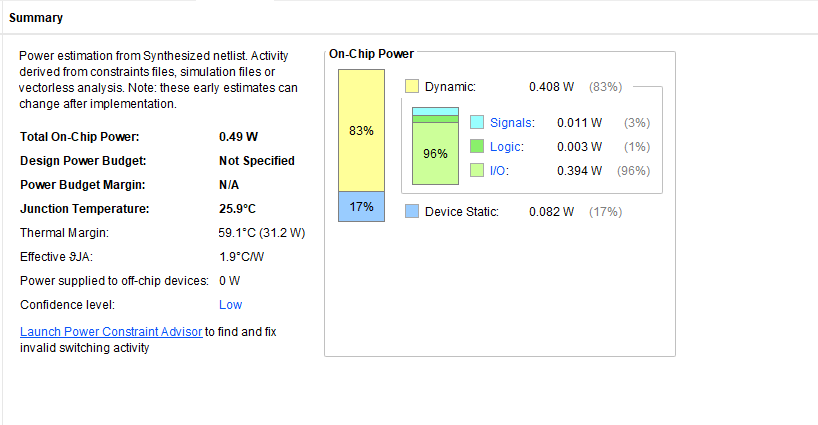
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

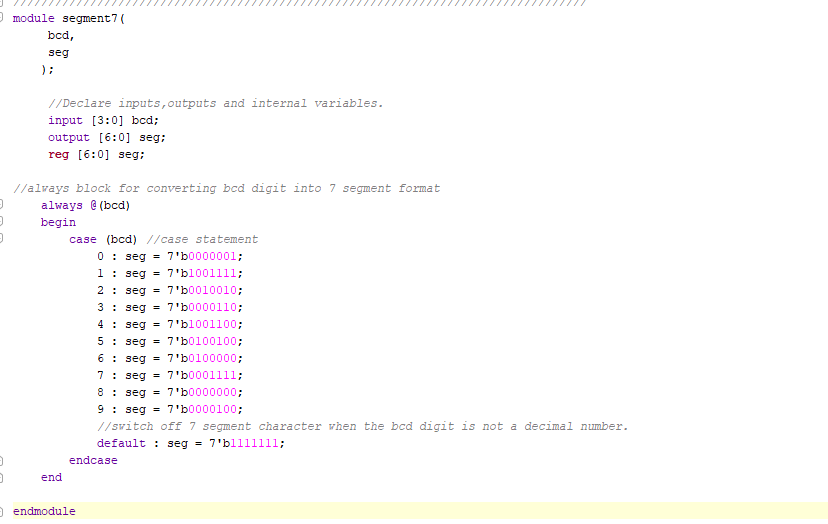


POWER REPORT:-

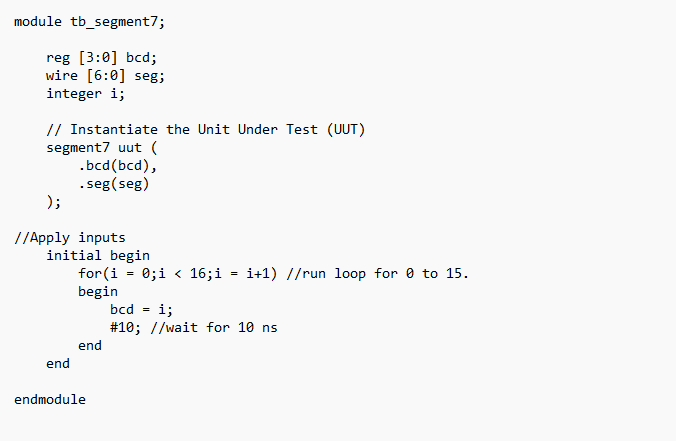


Q3. BCD TO SEVEN SEGMENT DISPLAY

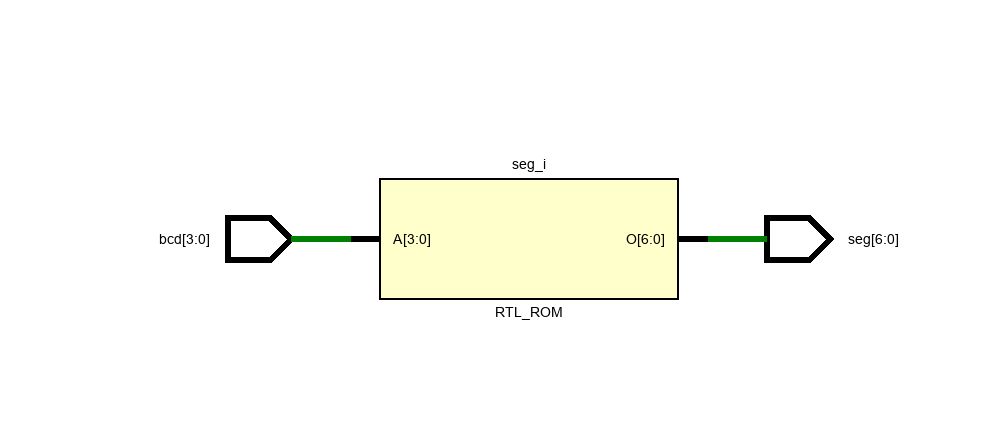
VERILOG CODE:-



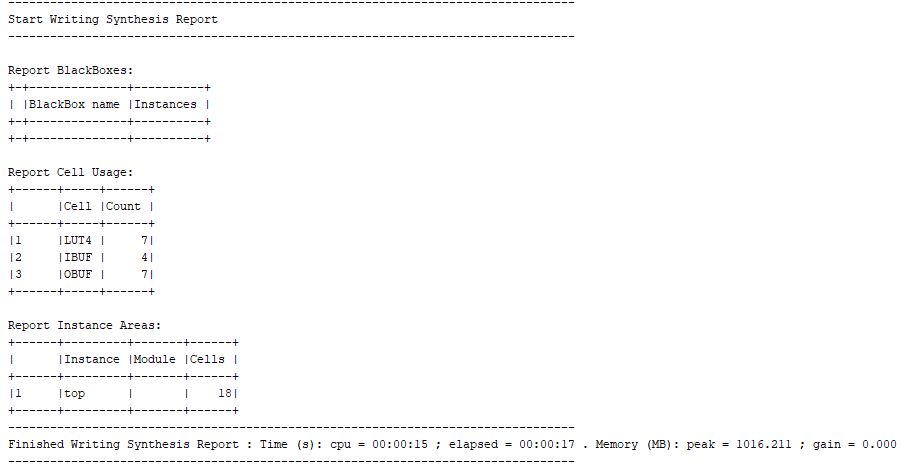
TESTBENCH:-



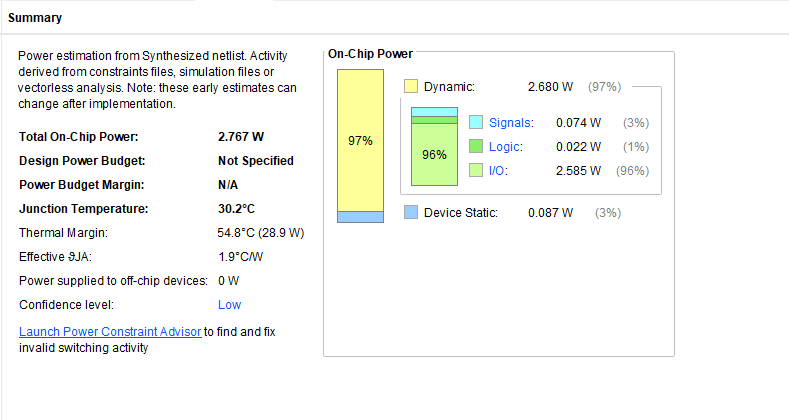
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

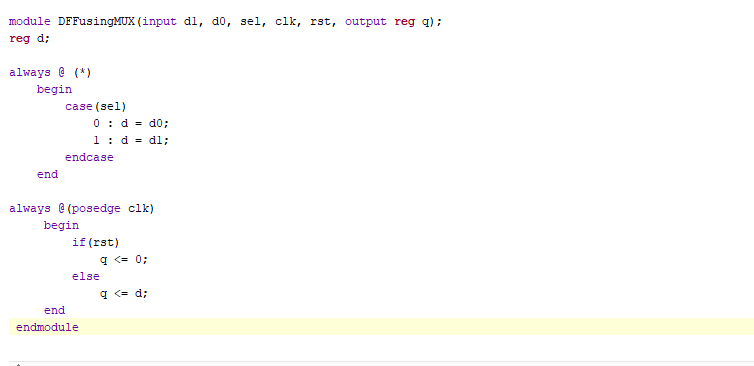


POWER REPORT:-

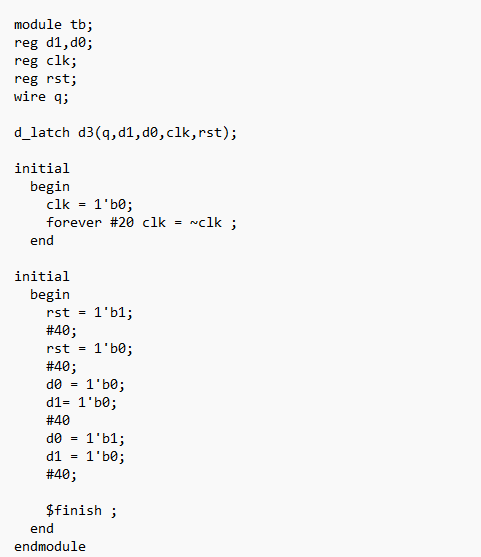


Q4. D LATCH USING 2:1 MUX

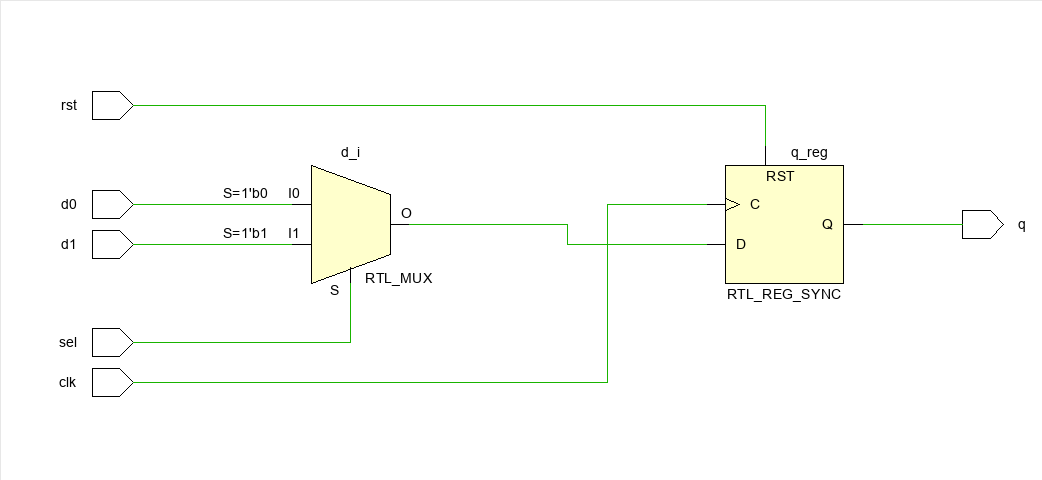
VERILOG CODE:-



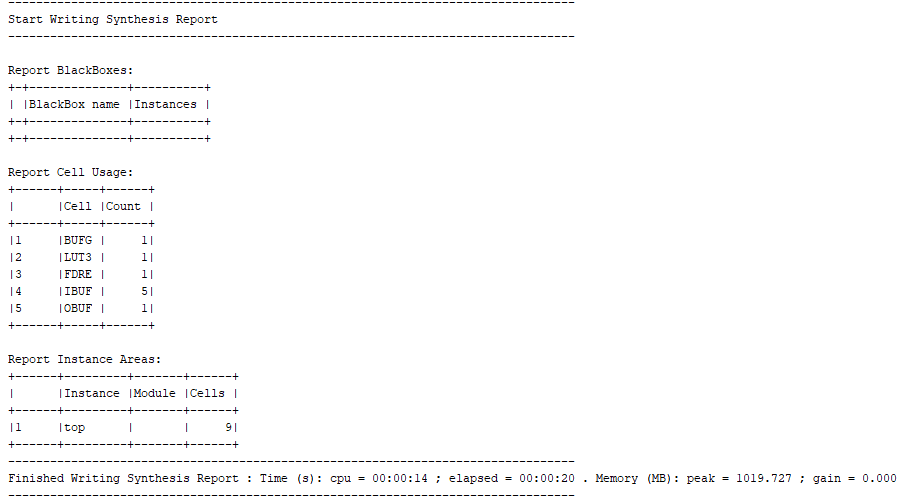
TESTBENCH:-



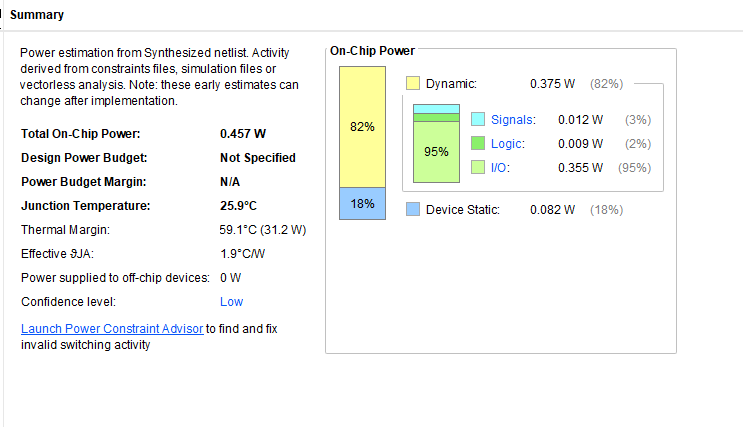
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

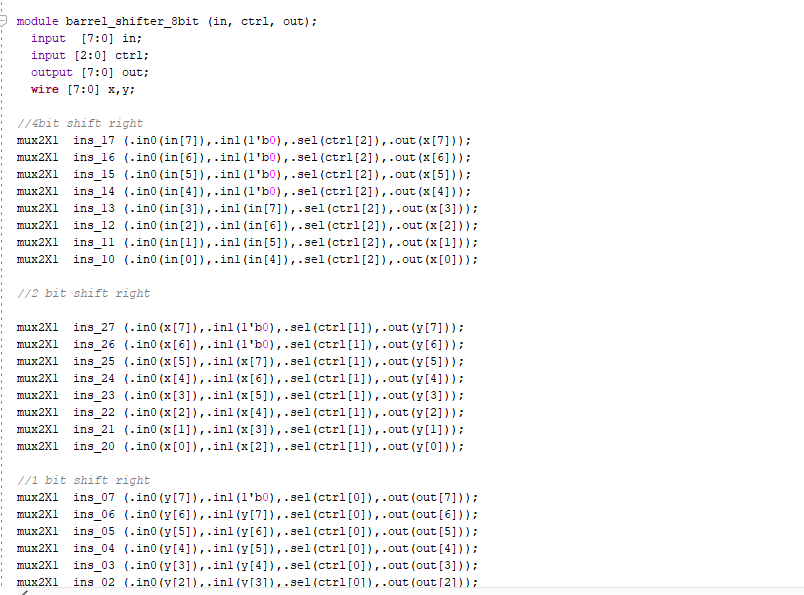


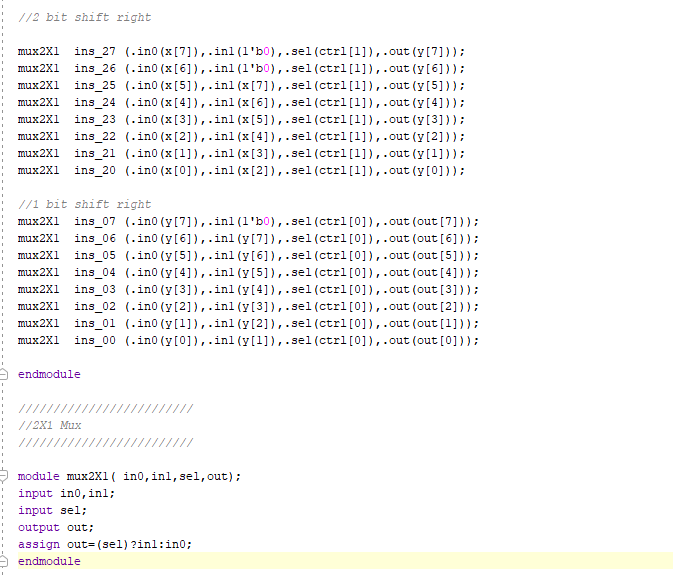
POWER REPORT:-



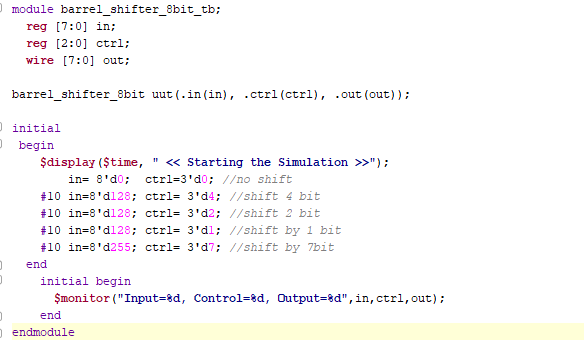
Q5. 8-BIT BARREL SHIFTER

VERILOG CODE:-

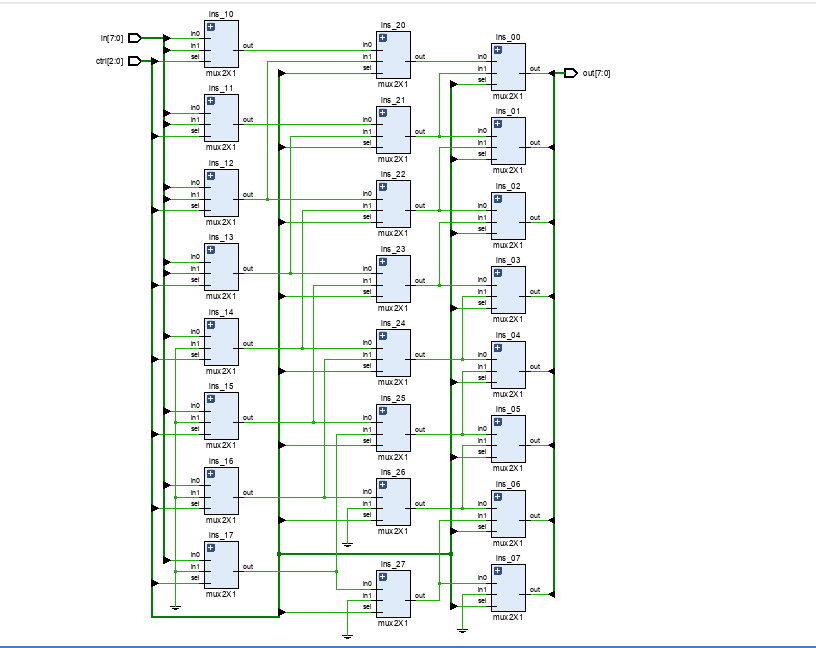




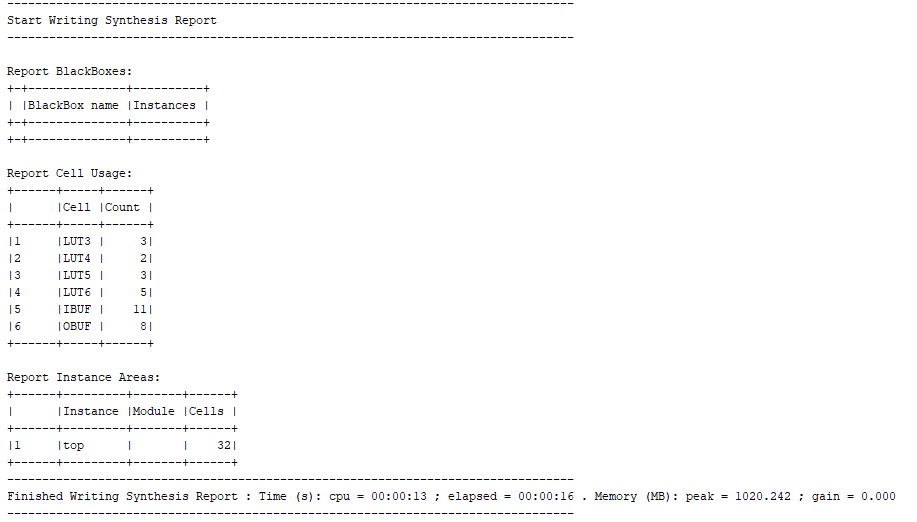
TESTBENCH:-



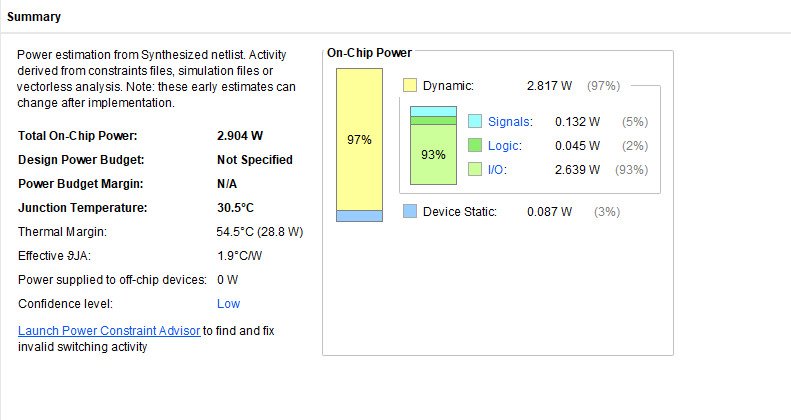
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

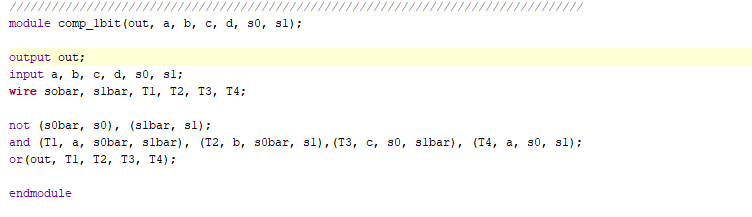


POWER REPORT:-

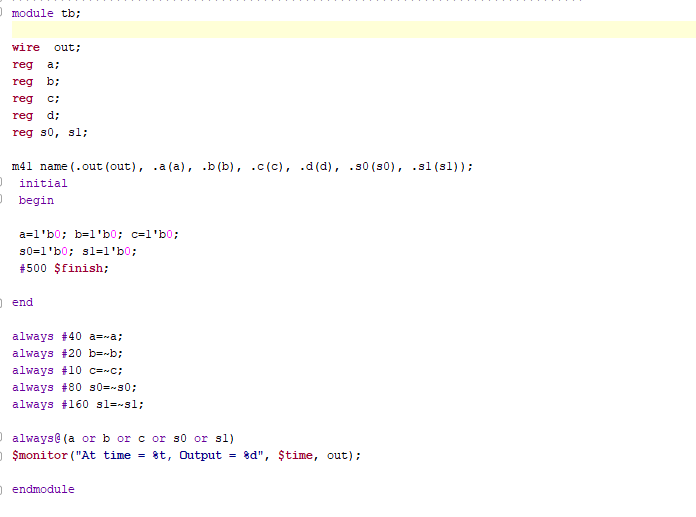


Q6. 1-BIT COMPARATOR USING 4X1 MUX

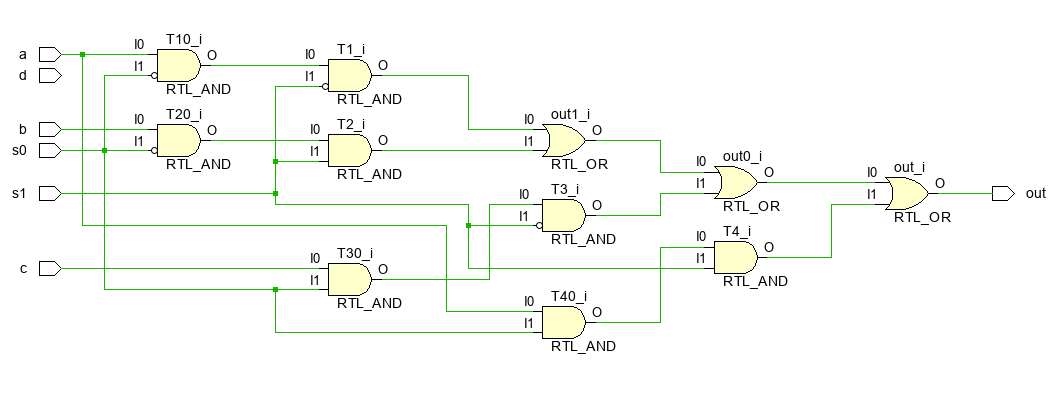
VERILOG CODE:-



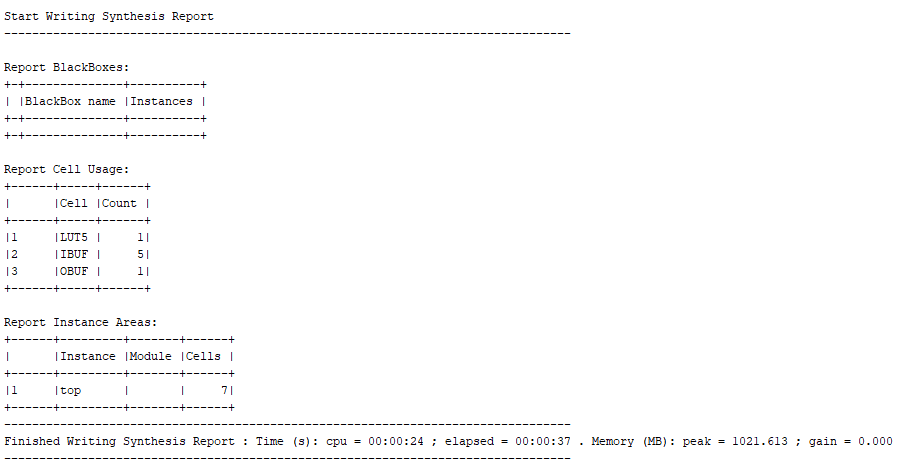
TESTBENCH:-



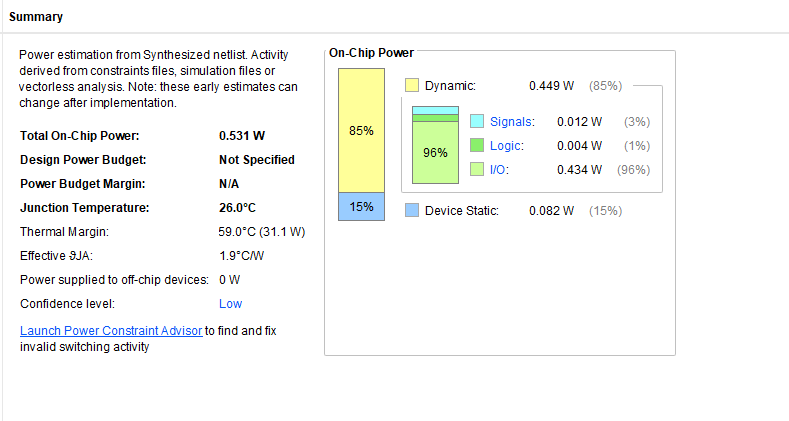
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

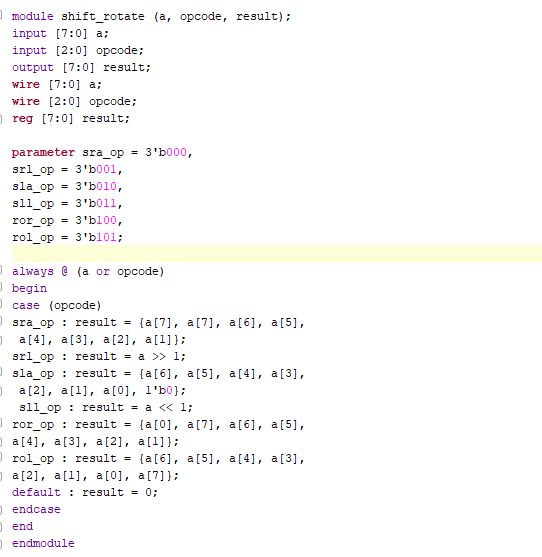


POWER REPORT:-



Q7.LOGICAL, ALGEBRAIC, AND ROTATE SHIFT OPERATIONS

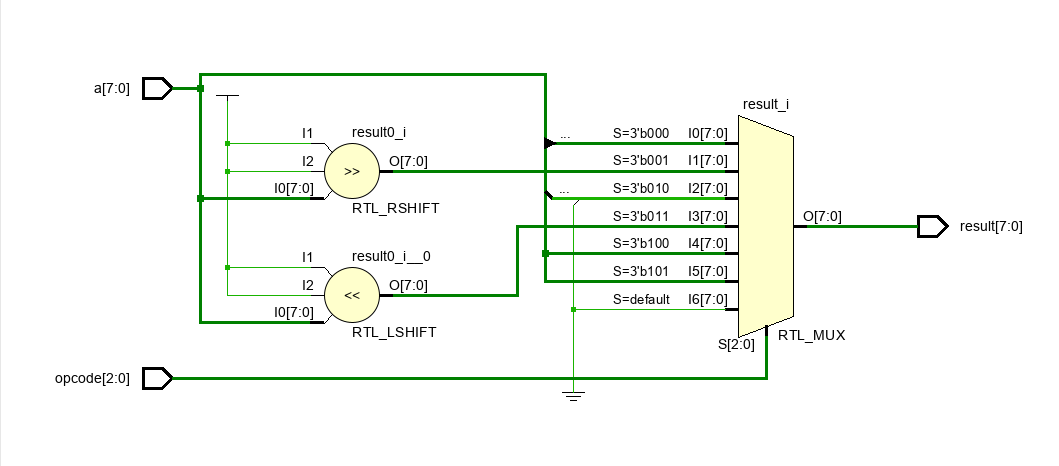
VERILOG CODE:-



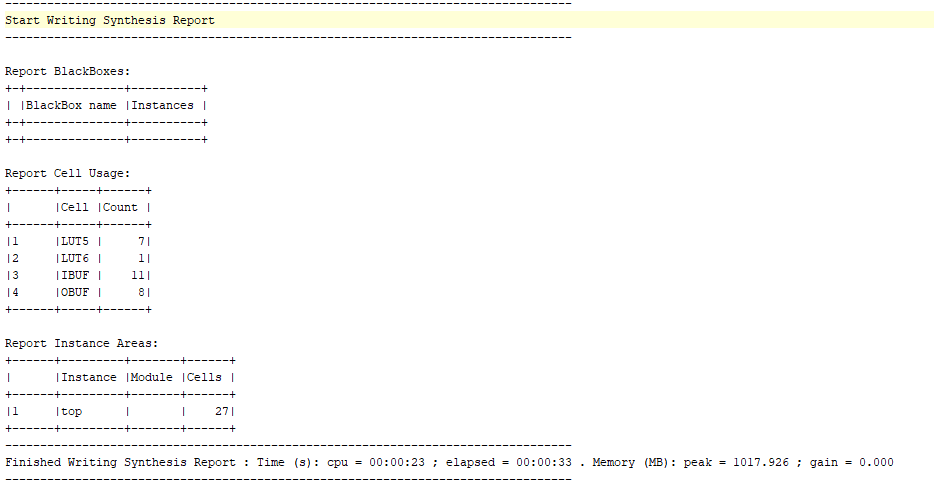
TESTBENCH:-



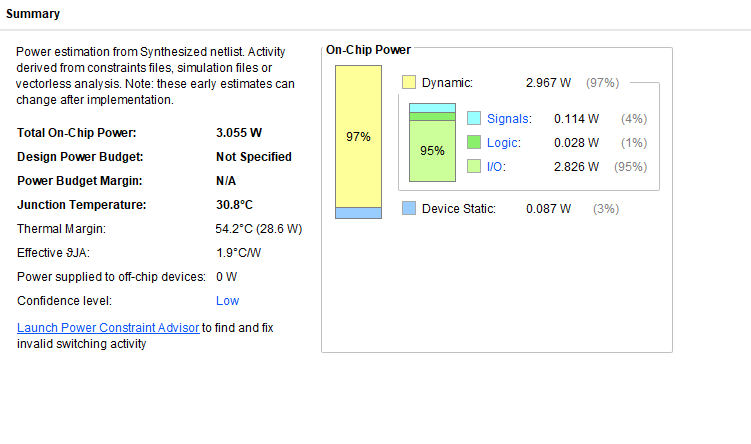
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

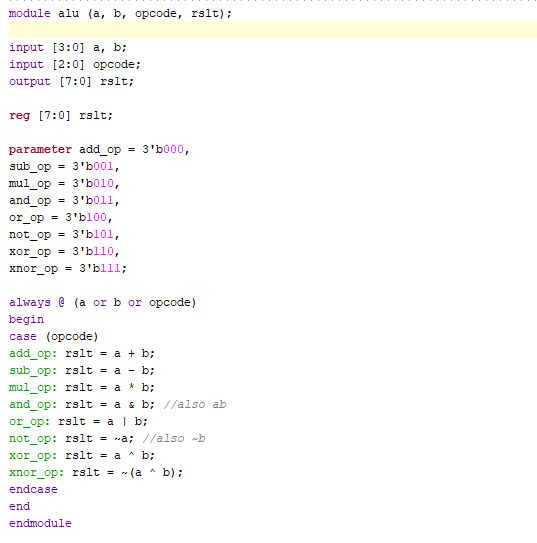


POWER REPORT:-

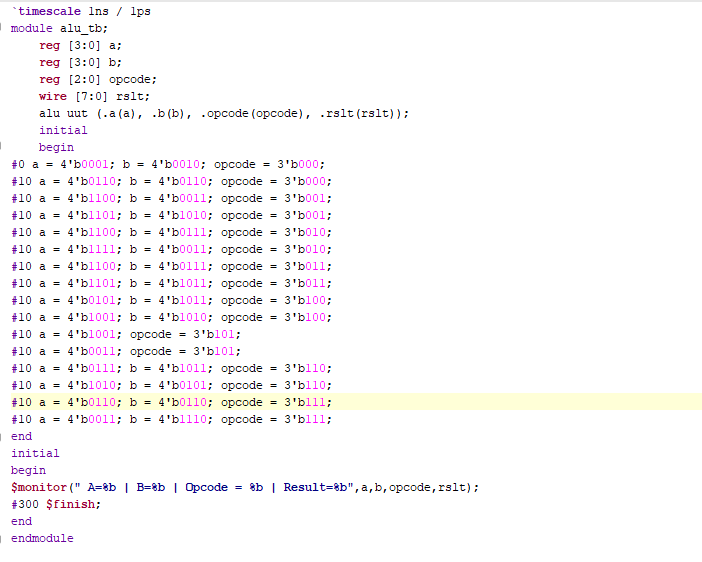


Q8. ALU

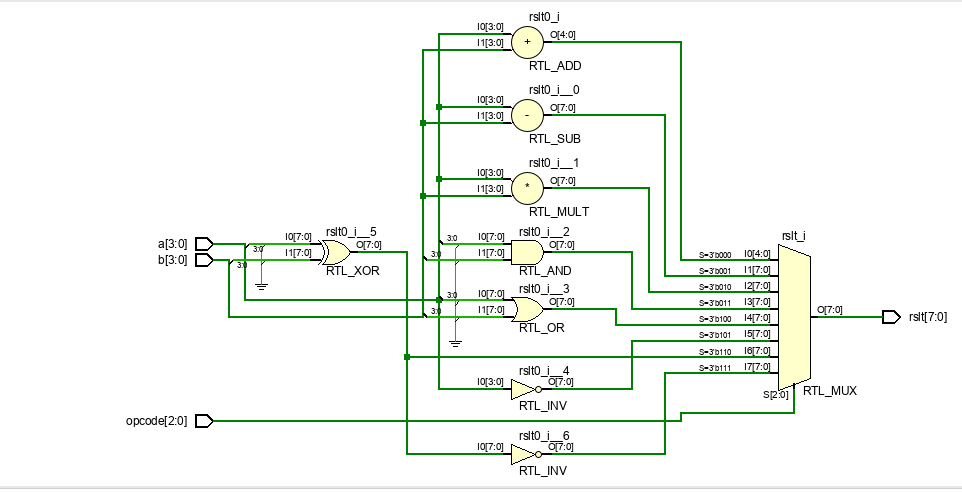
VERILOG CODE:-



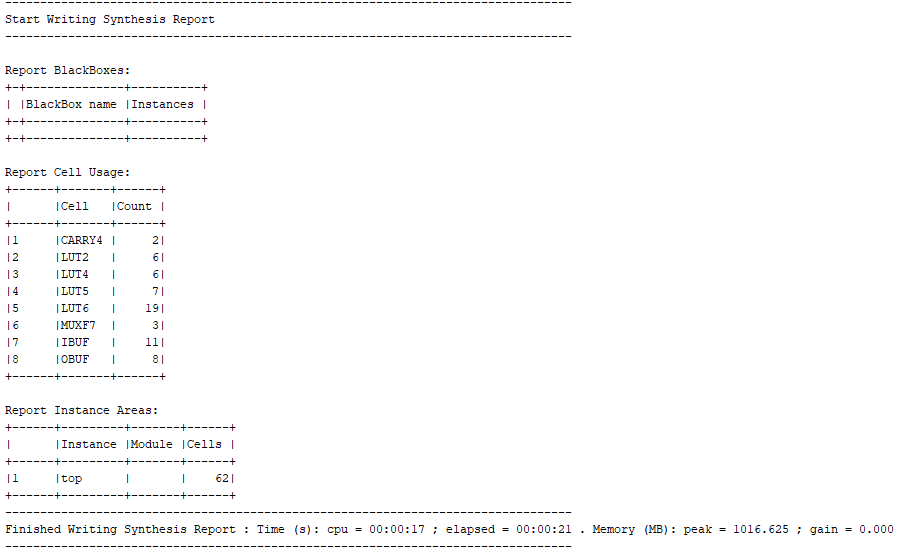
TEST BENCH:-



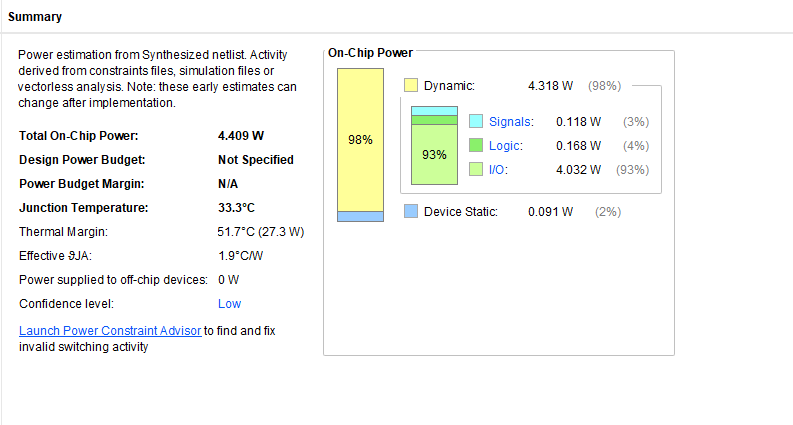
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

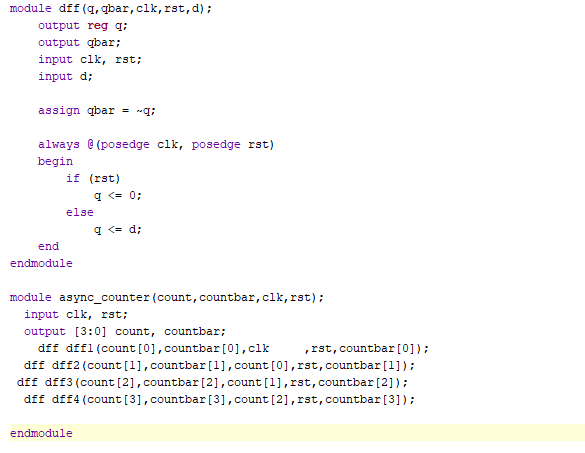


POWER REPORT:-

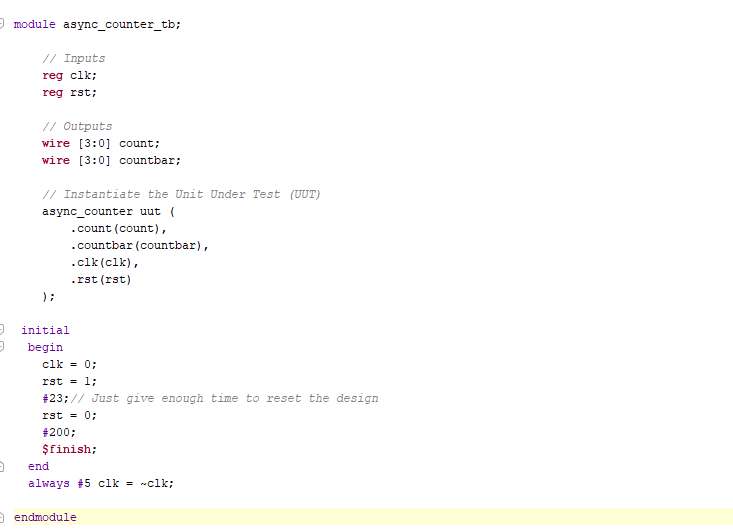


Q9. 4-BIT ASYNCHRONOUS DOWN COUNTER

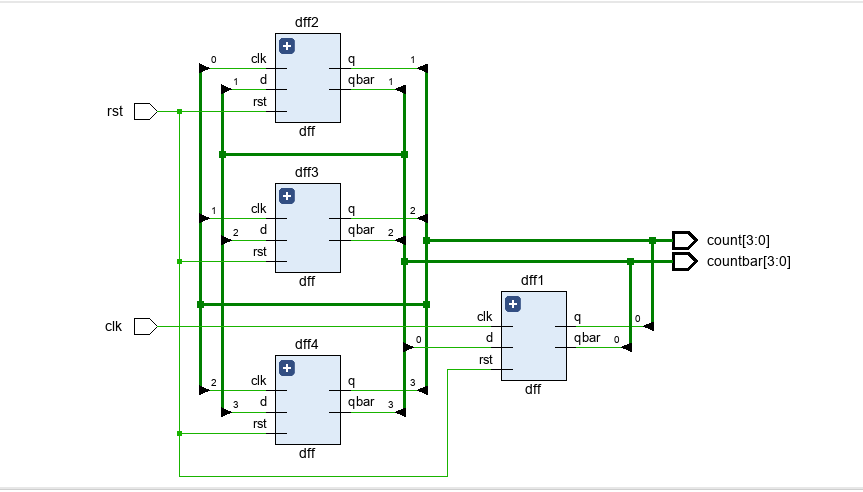
VERILOG CODE:-



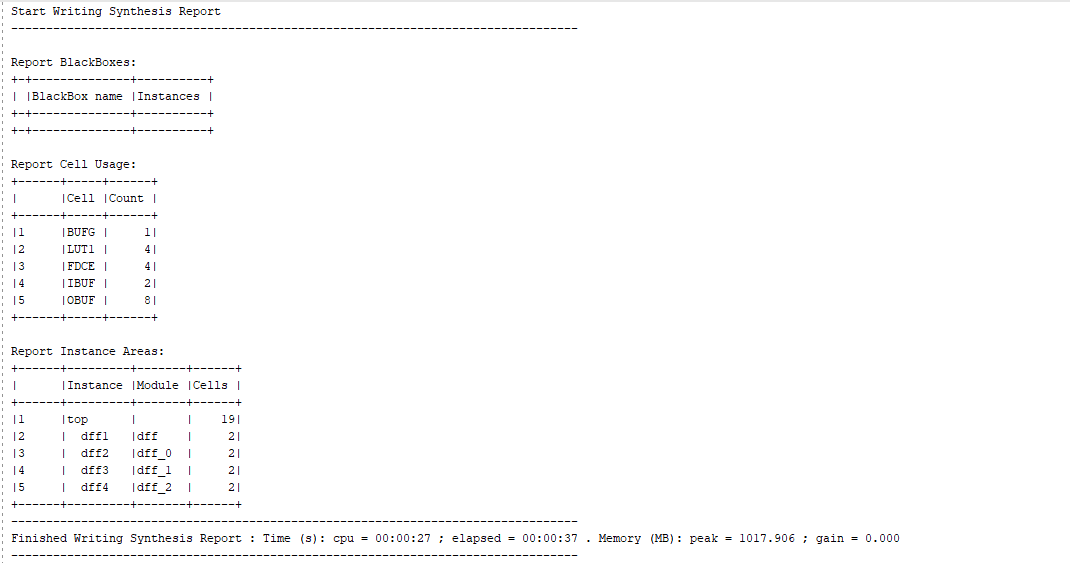
TESTBENCH:-



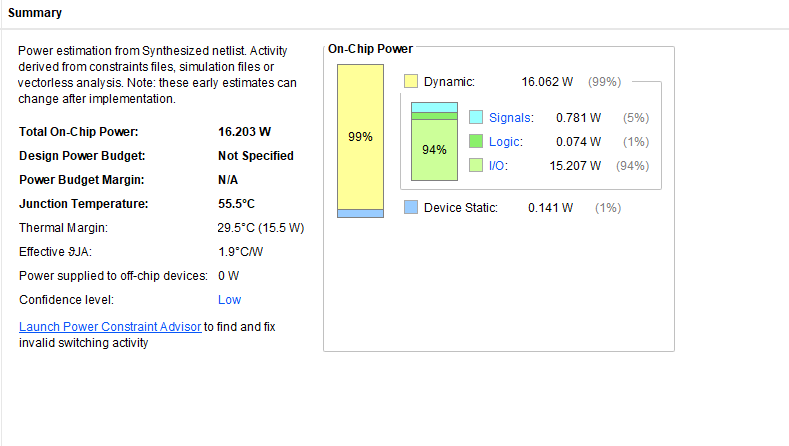
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

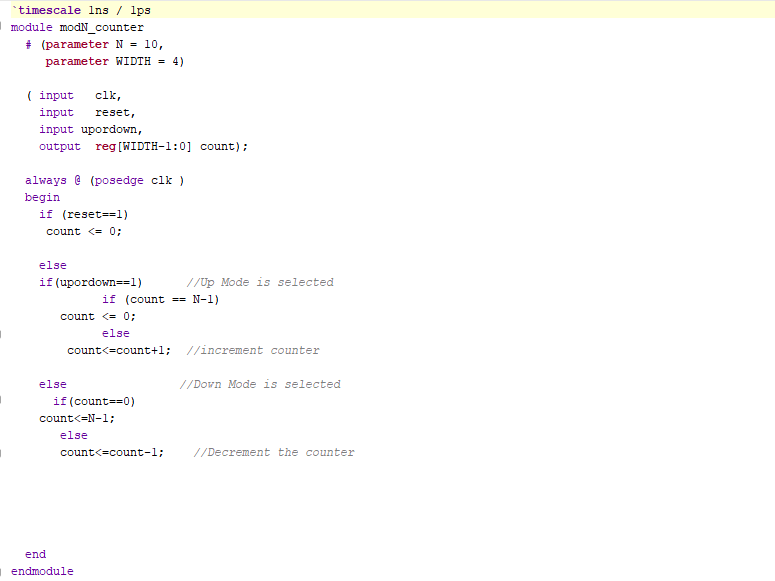


POWER REPORT:-

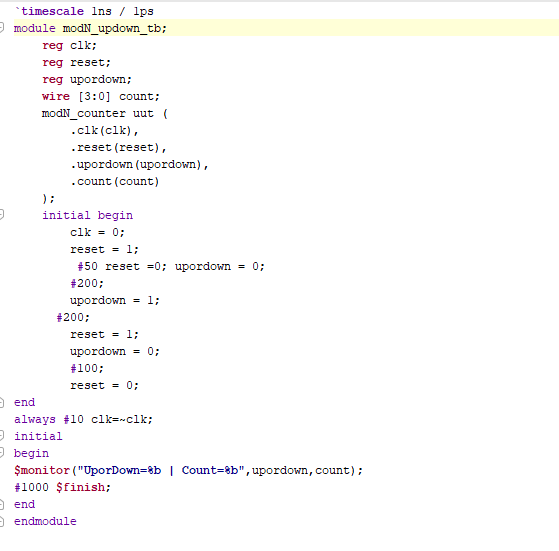


Q10. MOD-N UPDOWN COUNTER

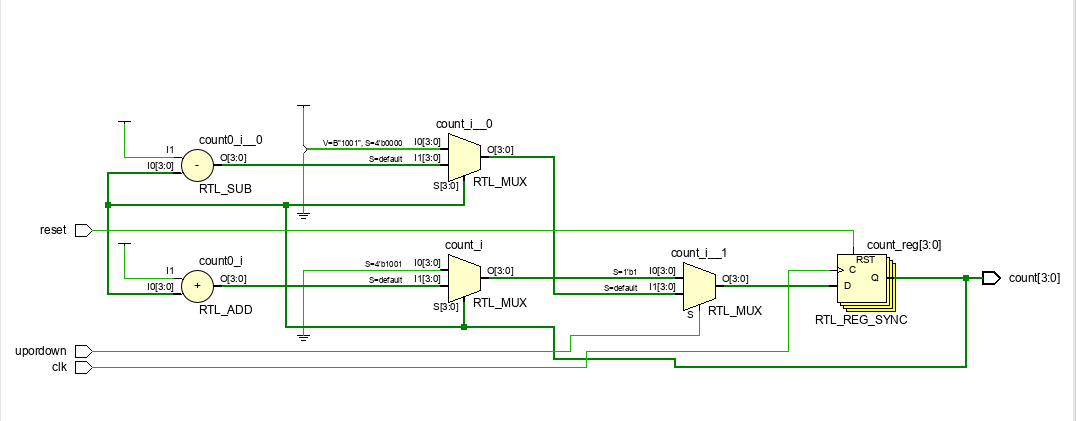
VERILOG CODE:-



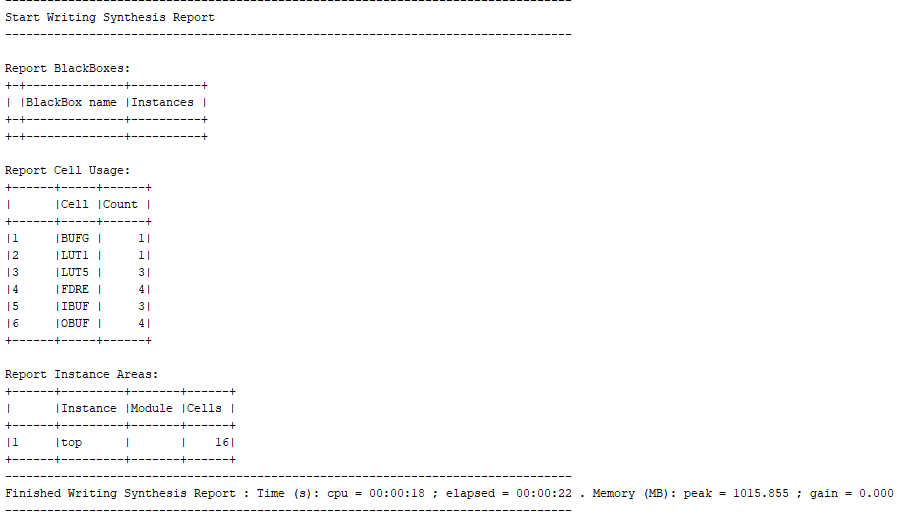
TESTBENCH:-



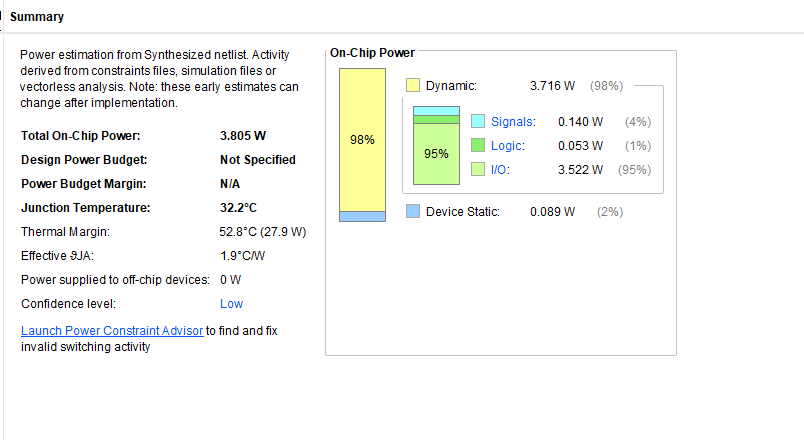
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

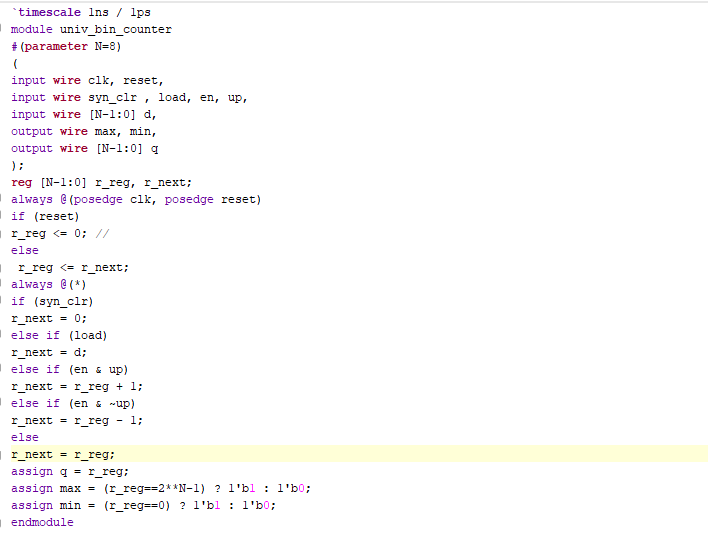


POWER REPORT:-

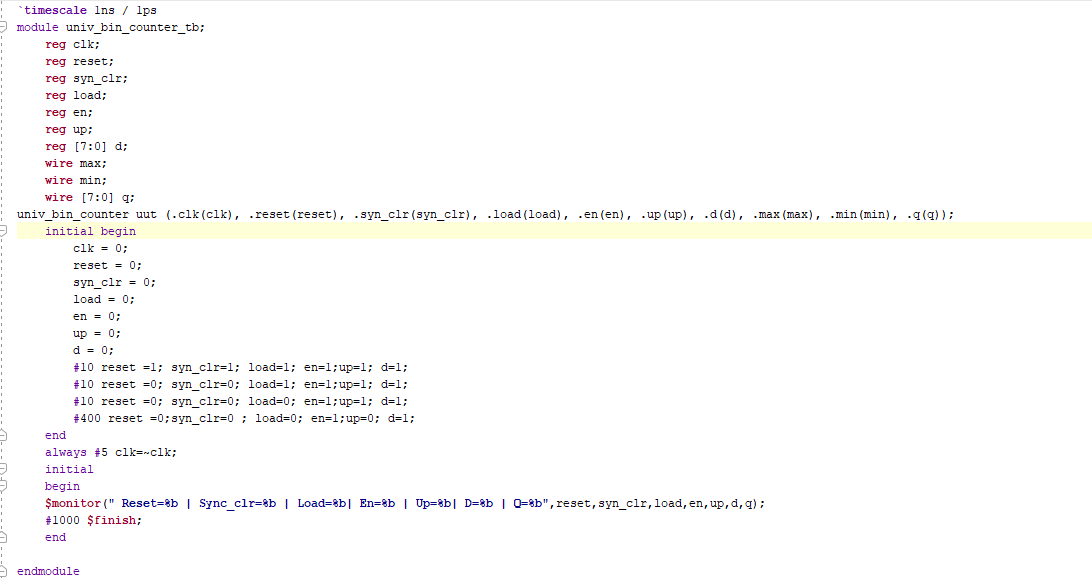


Q11. UNIVERSAL BINARY COUNTER

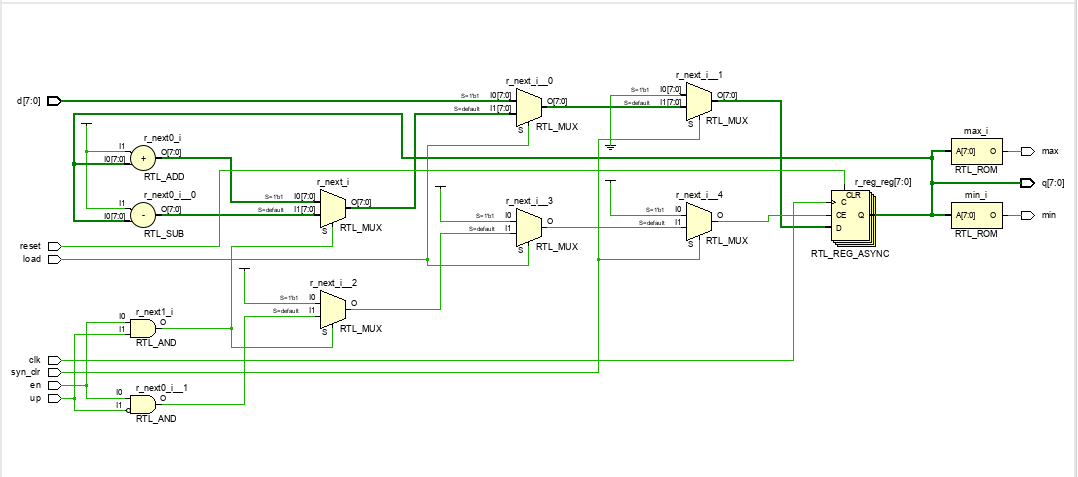
VERILOG CODE:-



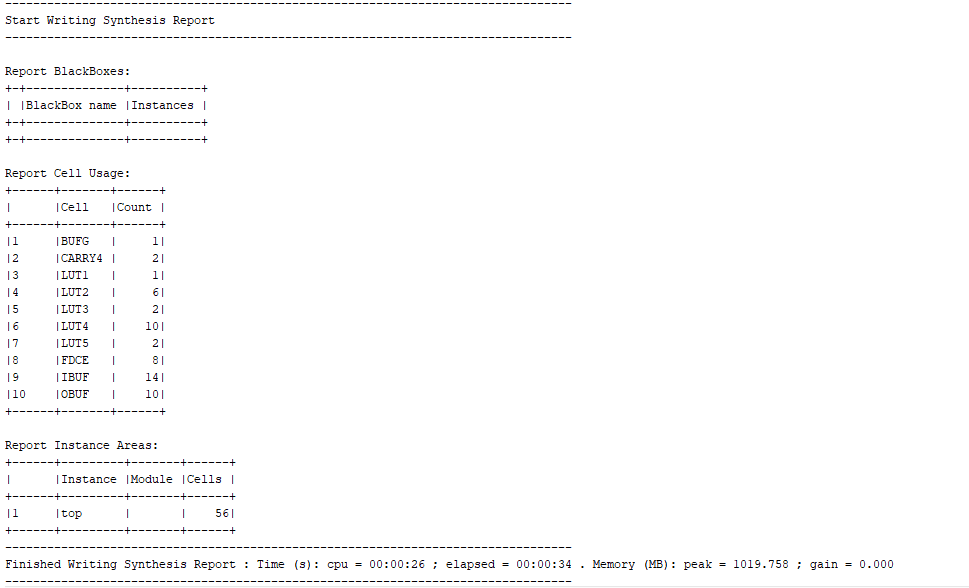
TESTBENCH:-



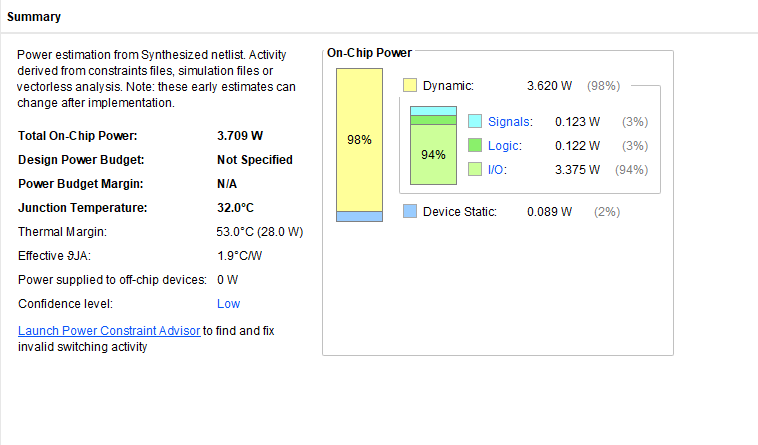
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

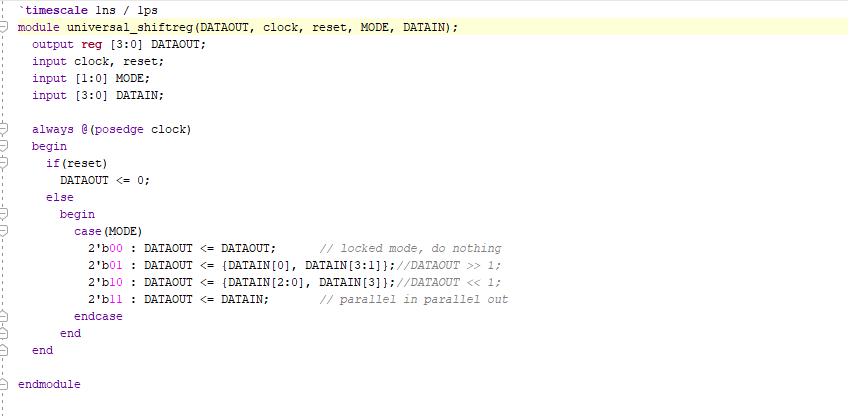


POWER REPORT:-

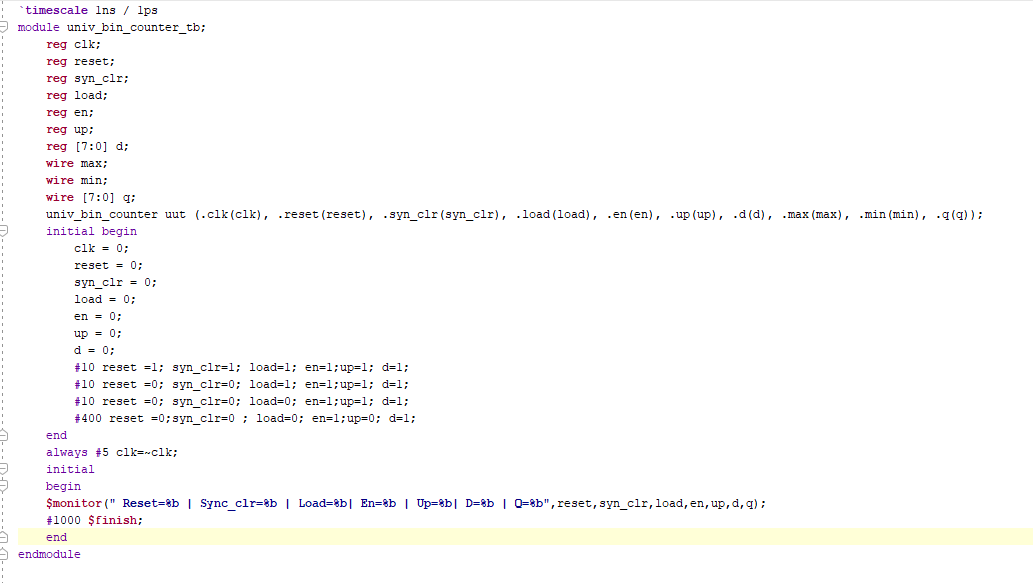


Q12. UNIVERSAL SHIFT REGISTER

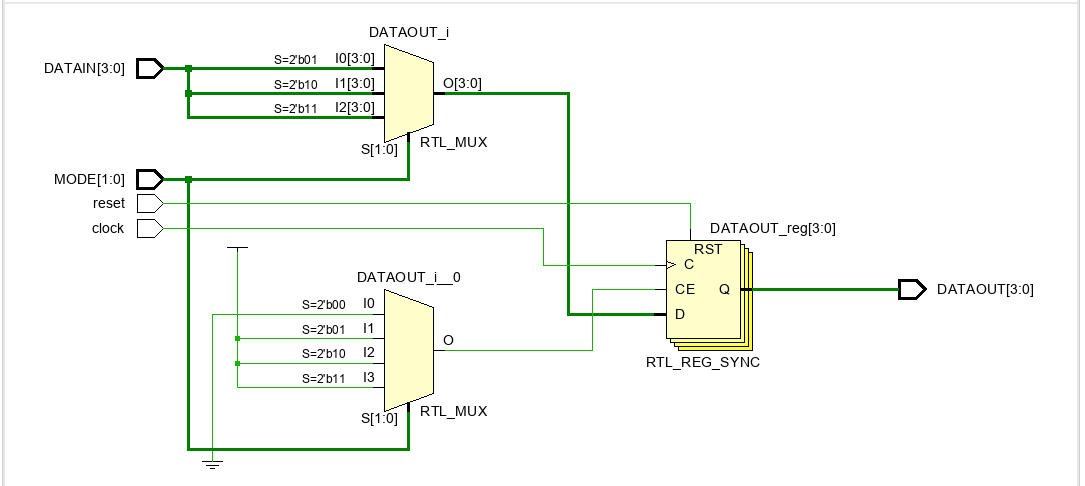
VERILOG CODE:-



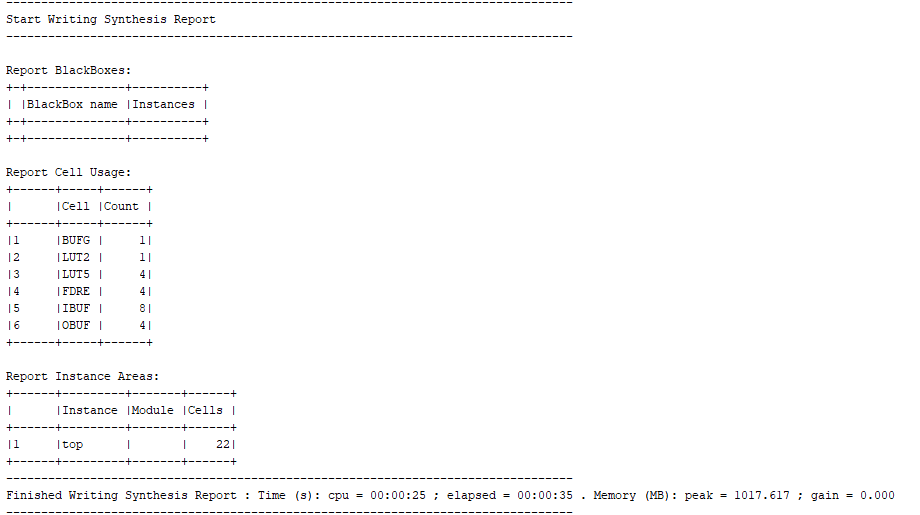
TESTBENCH:-



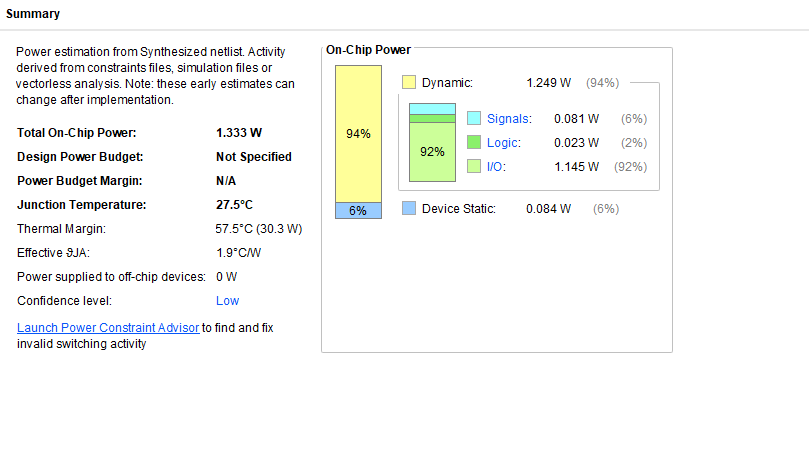
RTL SCHEMATIC:-



SYNTHESIS REPORT:-



POWER REPORT:-

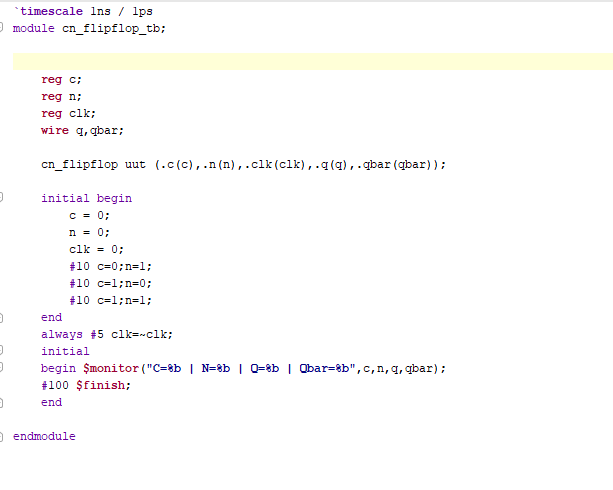


Q13. CN( CHANGE-NO CHANGE FLIPFLOP) USING 2:1 MUX

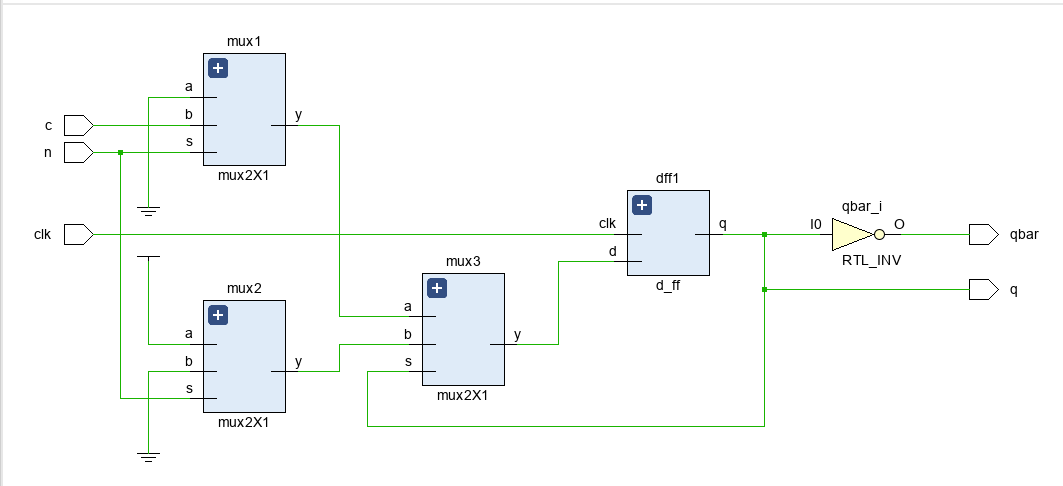
VERILOG CODE:-



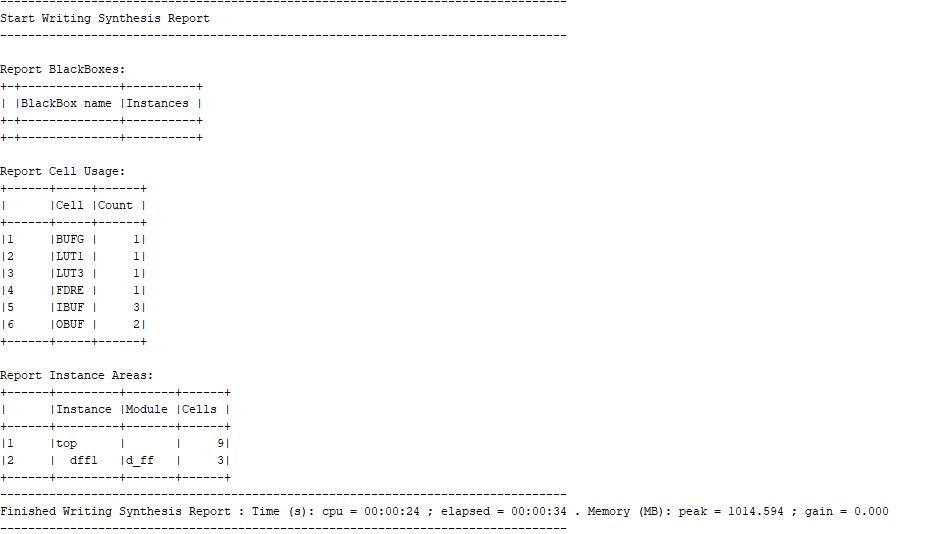
TESTBENCH:-



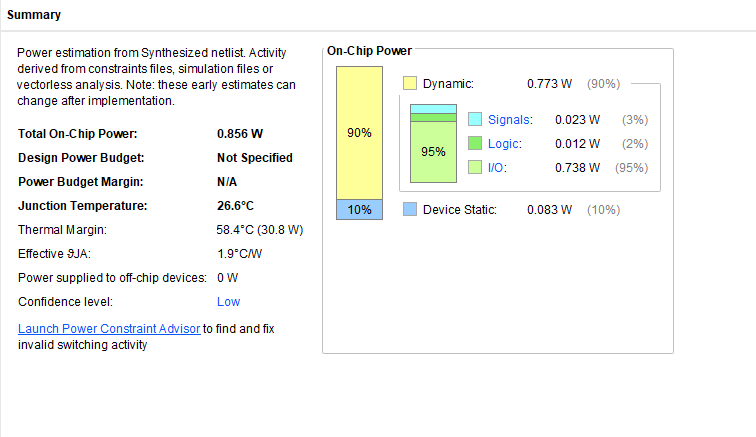
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

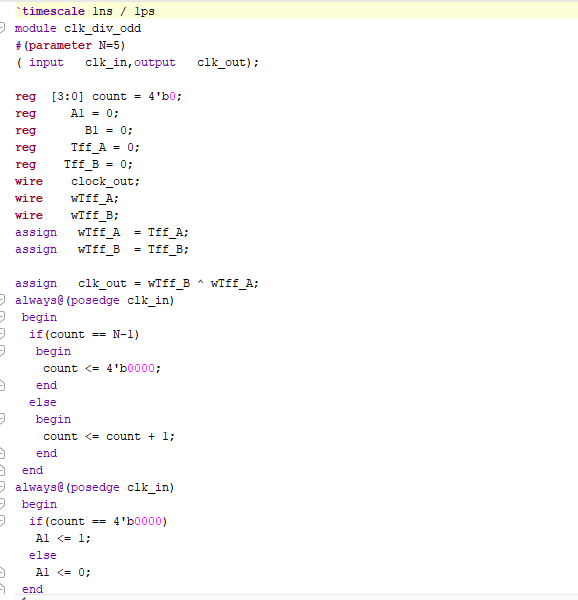


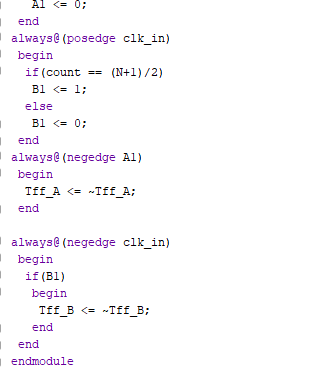
POWER REPORT:-



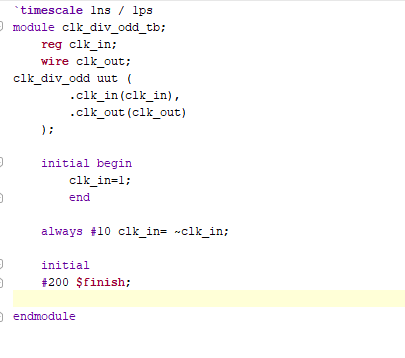
Q14.FREQUENCY DIVIDER BY ODD NUMBERS

VERILOG CODE:-

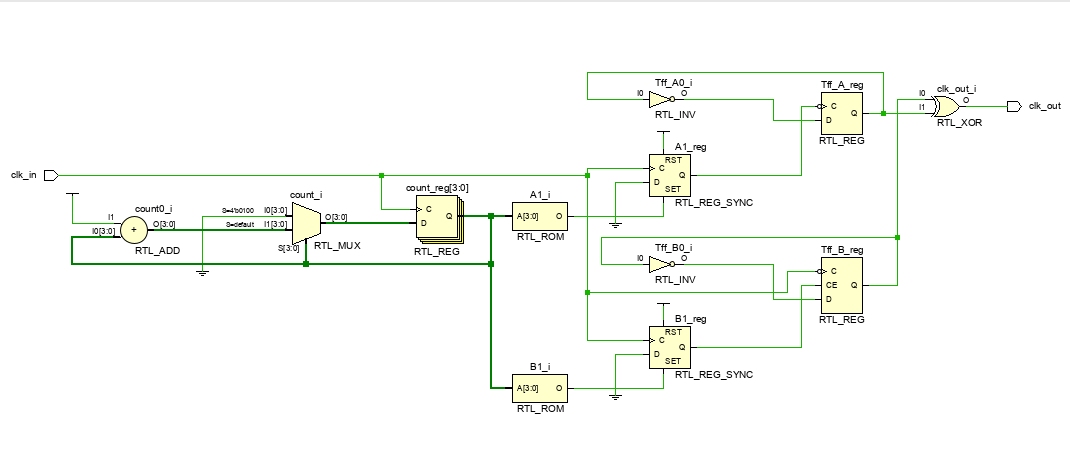




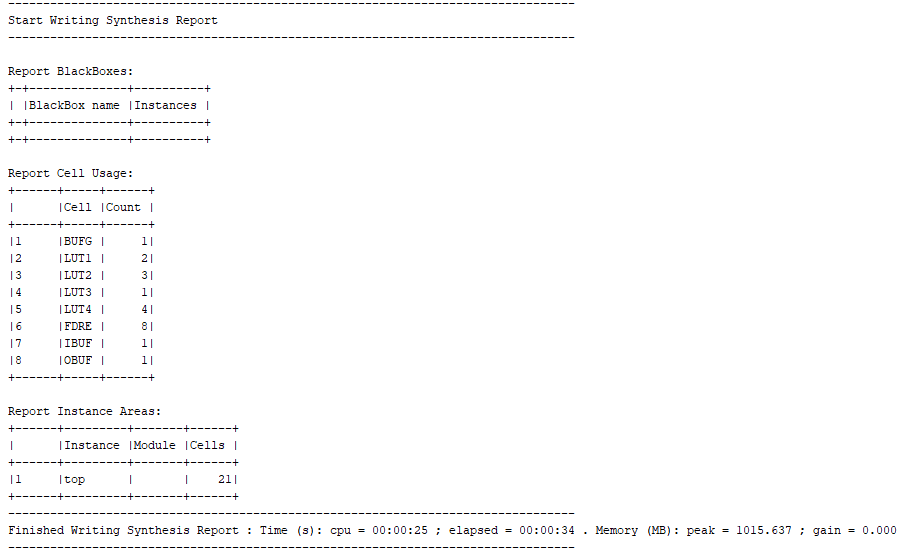
TESTBENCH:-



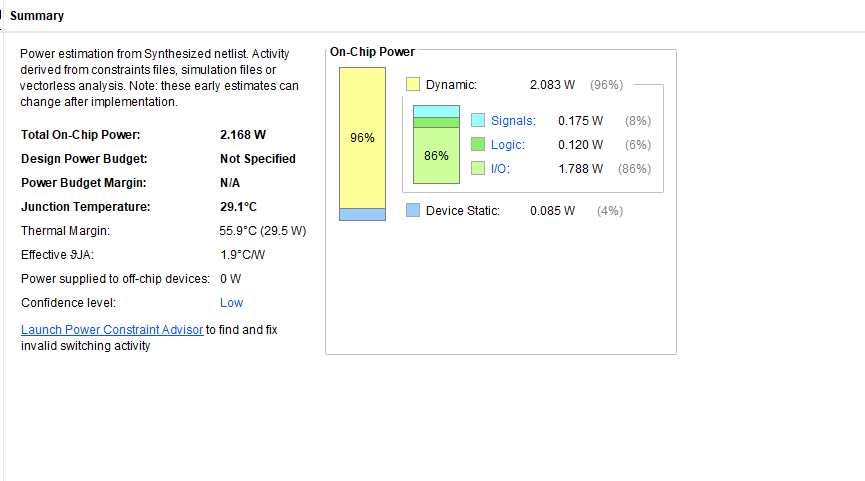
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

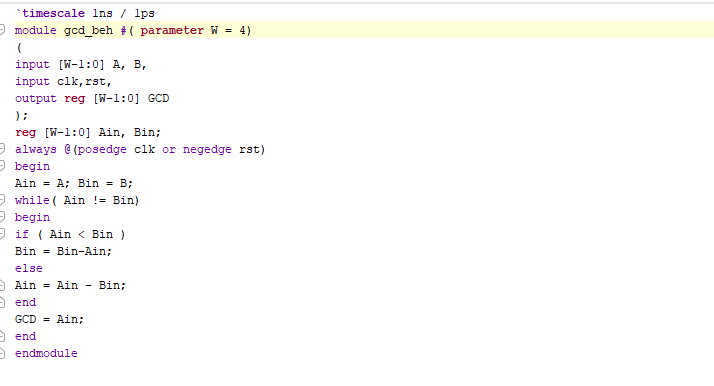


POWER REPORT:-

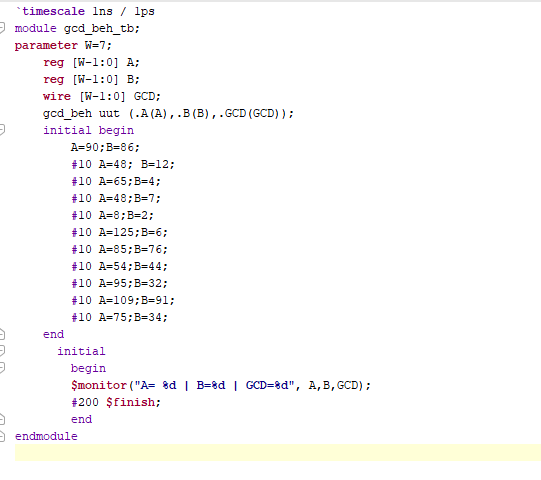


Q15. GREATEST COMMON DIVISOR USING BEHAVIOURAL MODELLING

VERILOG CODE:-

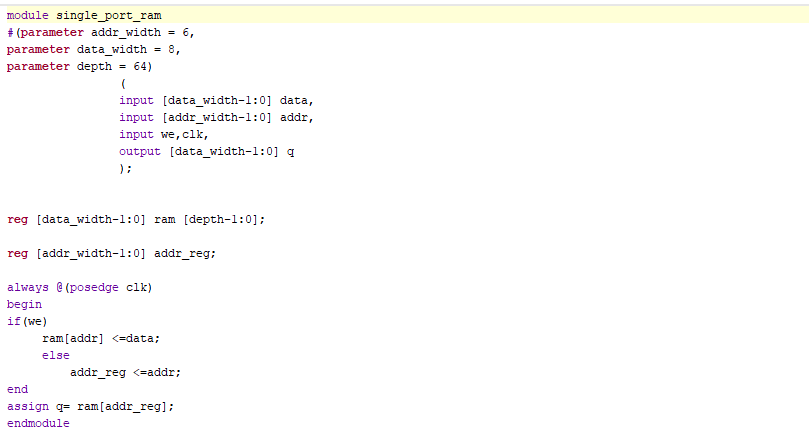


TESTBENCH:-

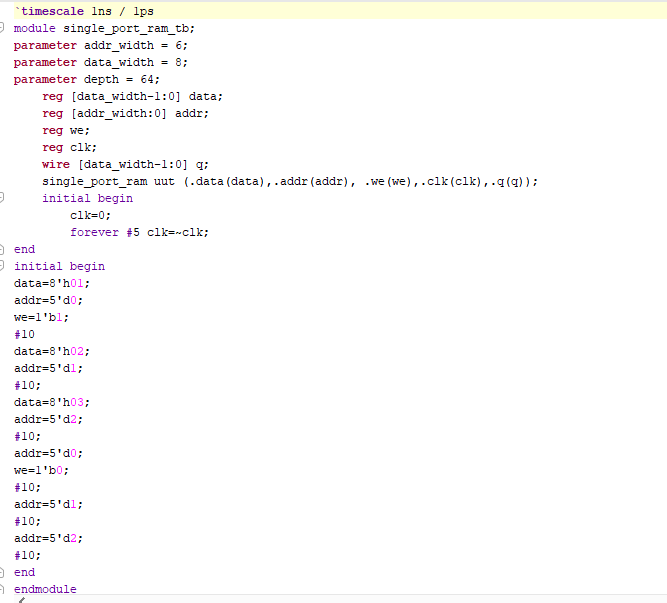


Q16.SINGLE PORT RAM

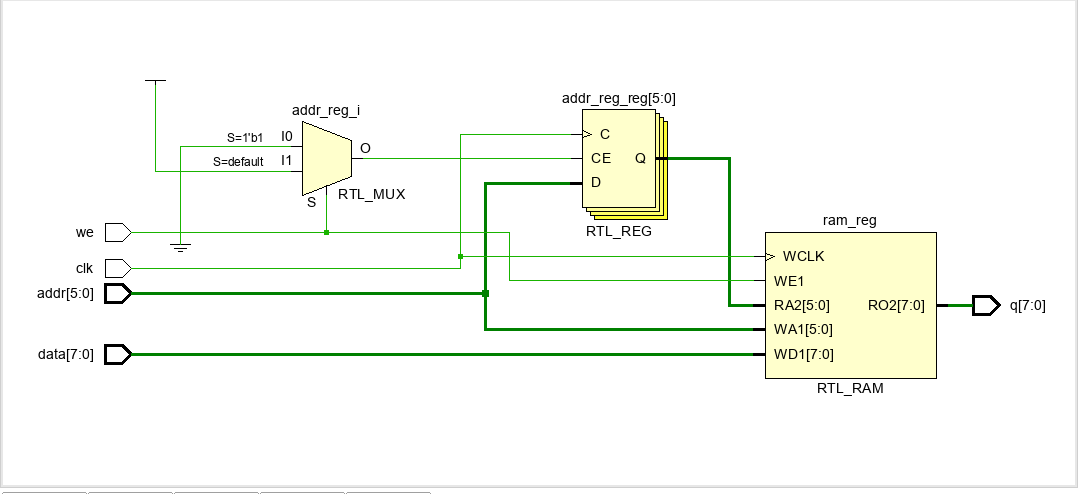
VERILOG CODE:-



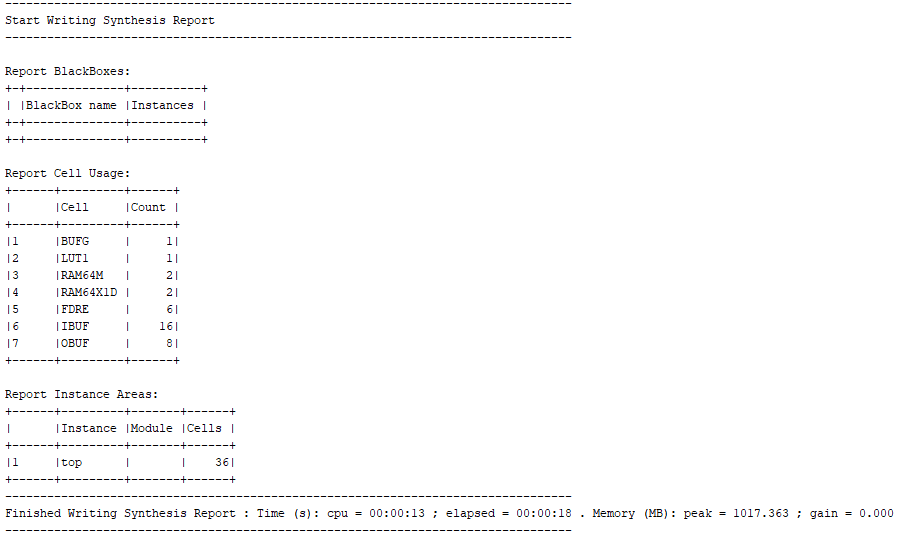
TESTBENCH:-



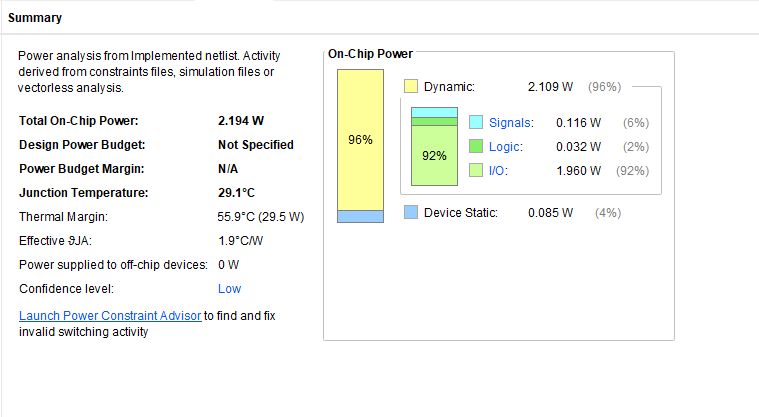
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

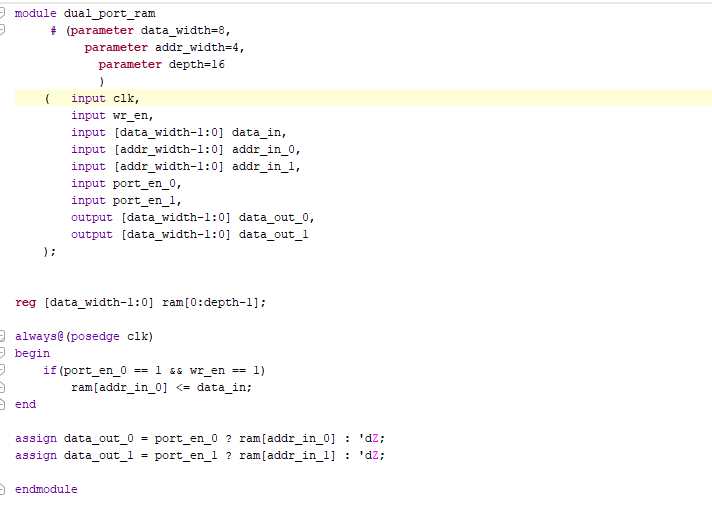


POWER REPORT:-

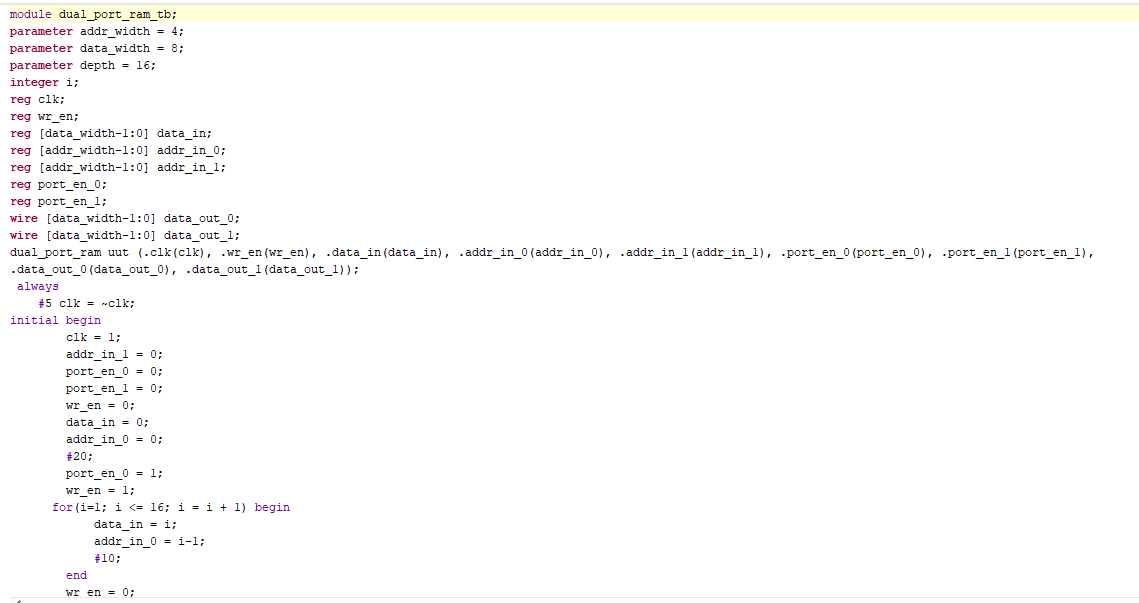


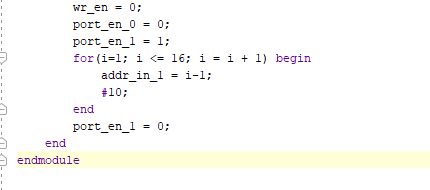
Q17. DUAL PORT RAM

VERILOG CODE:-

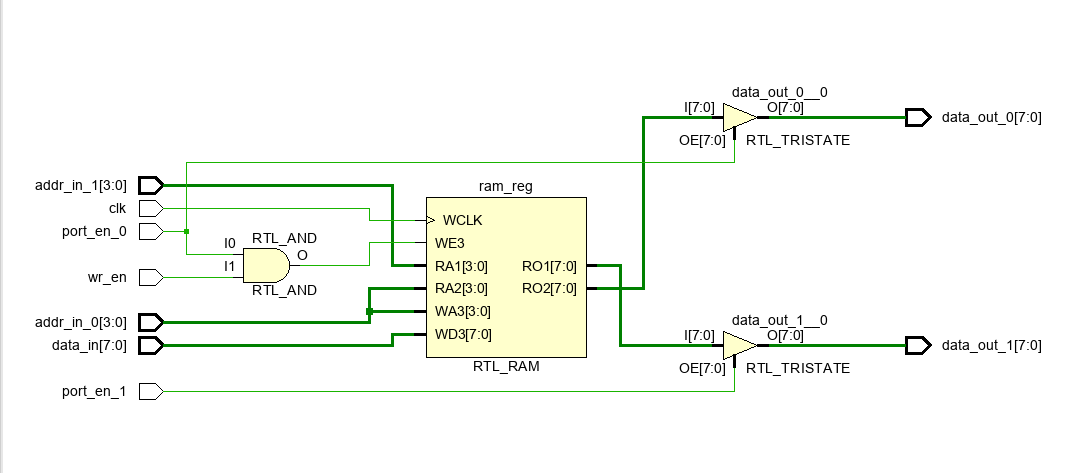


TESTBENCH:-

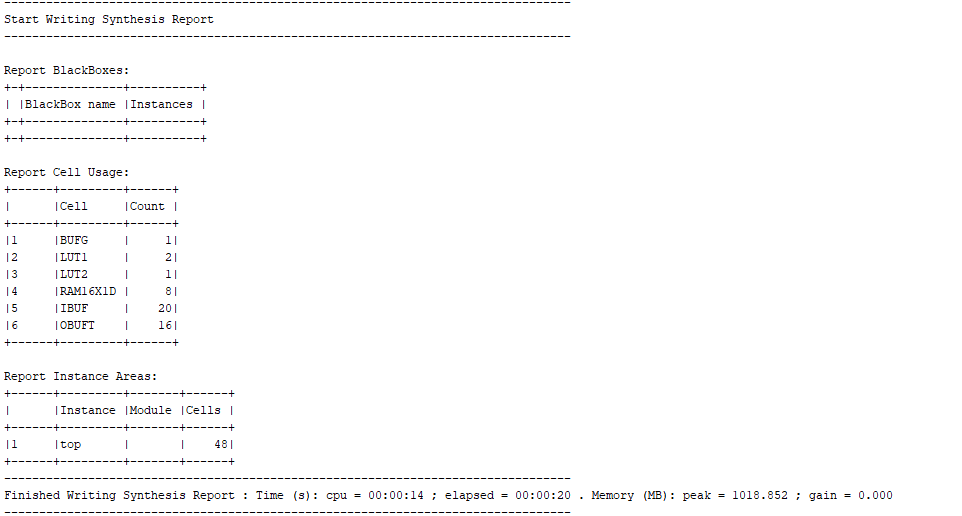




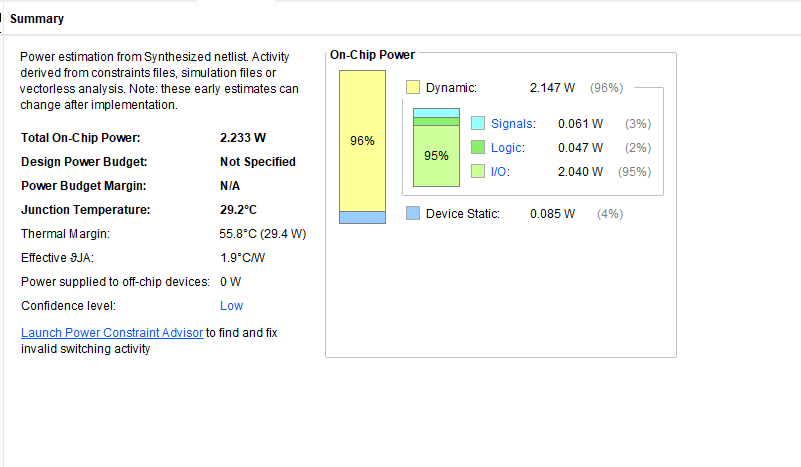
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

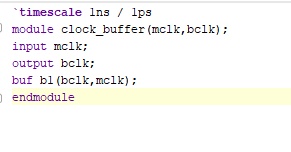


POWER REPORT:-



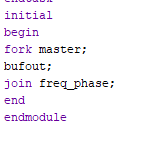
Q18. CLOCK BUFFER

VERILOG CODE:-

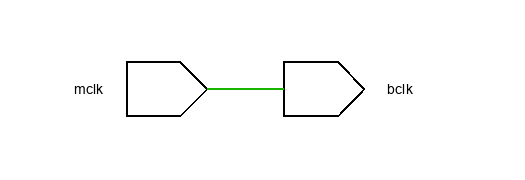


TESTBENCH:-

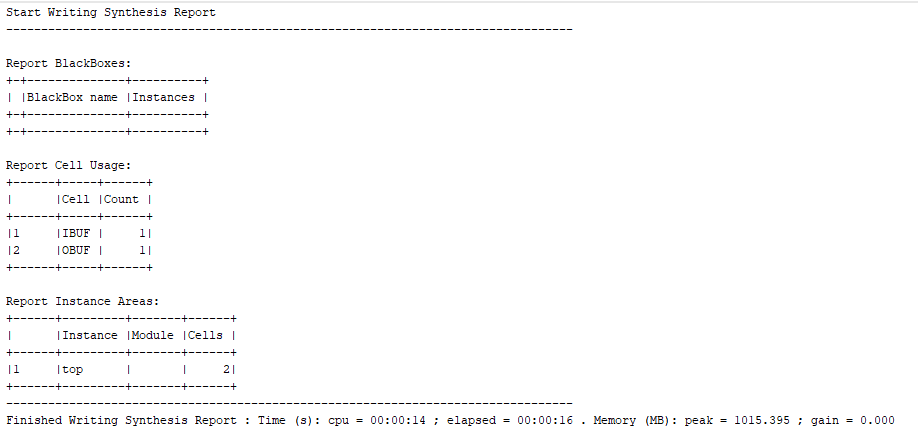




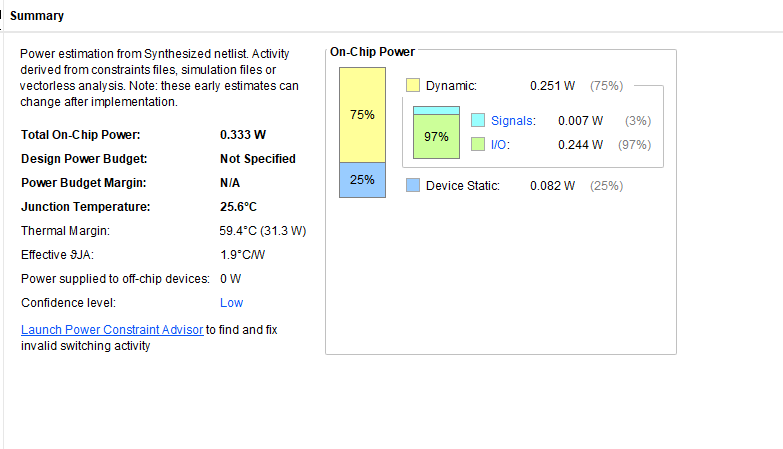
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

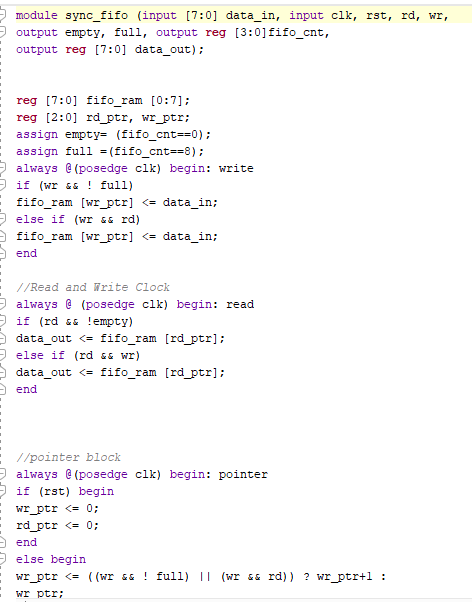


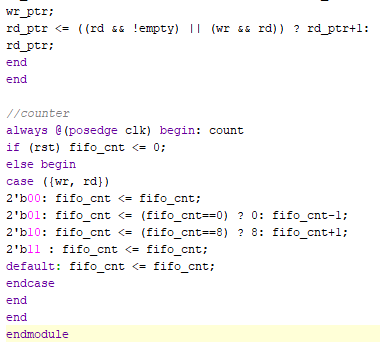
POWER REPORT:-



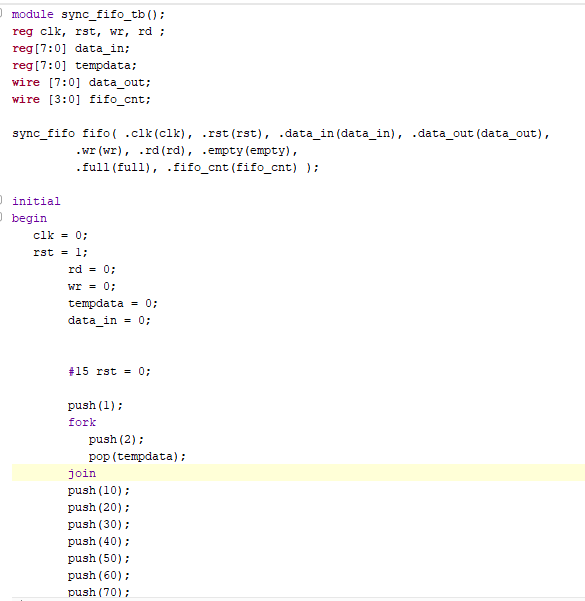
Q19. SYNCHRONOUS FIFO

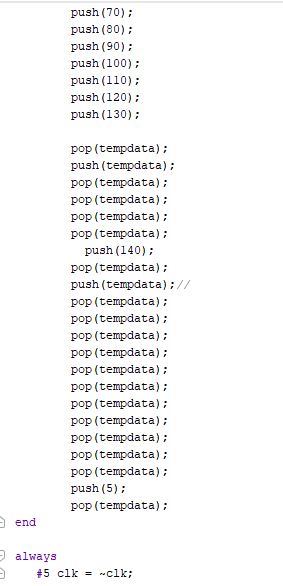
VERILOG CODE:-

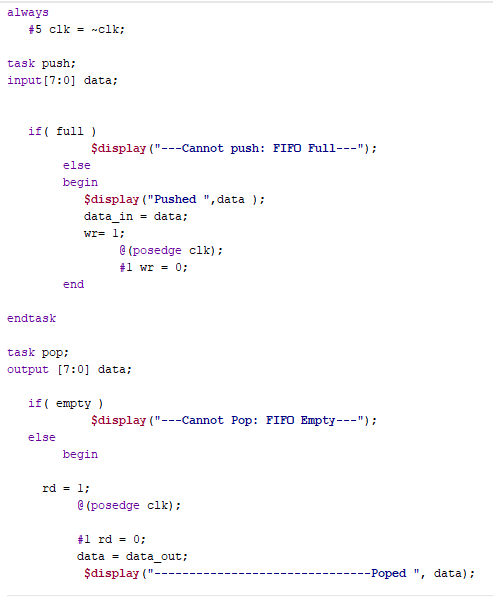


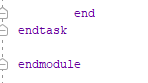


TESTBENCH:-

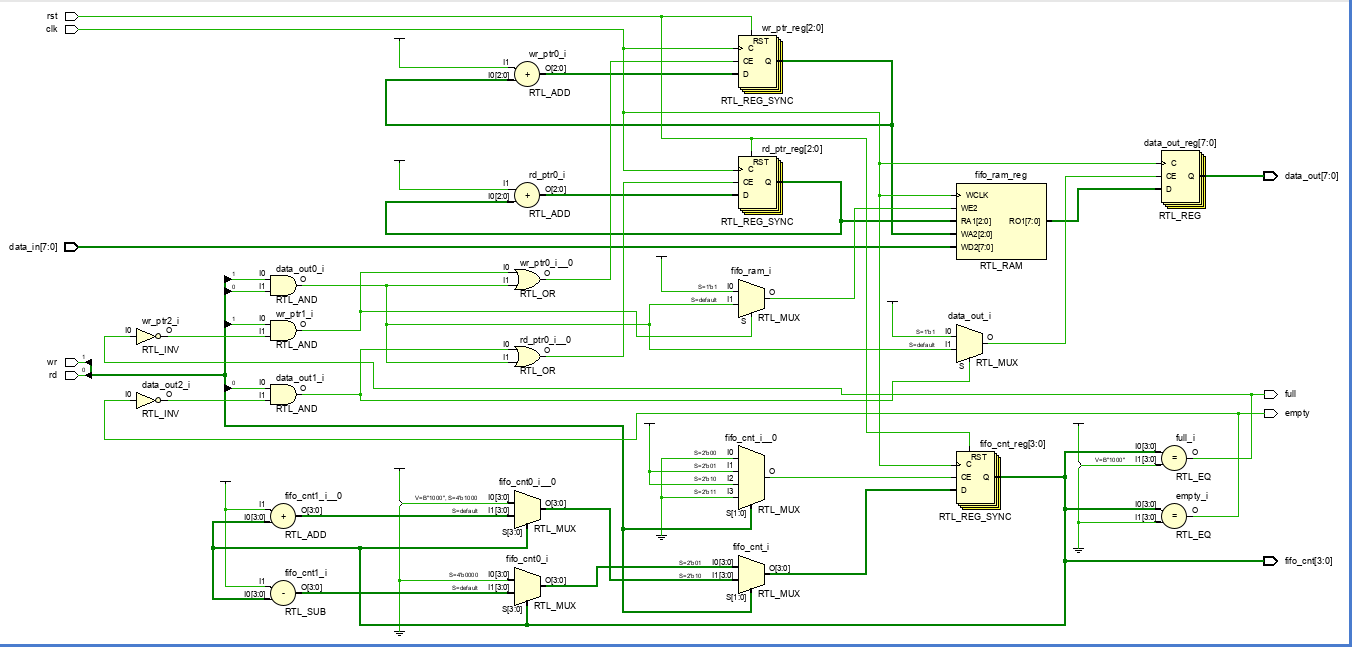








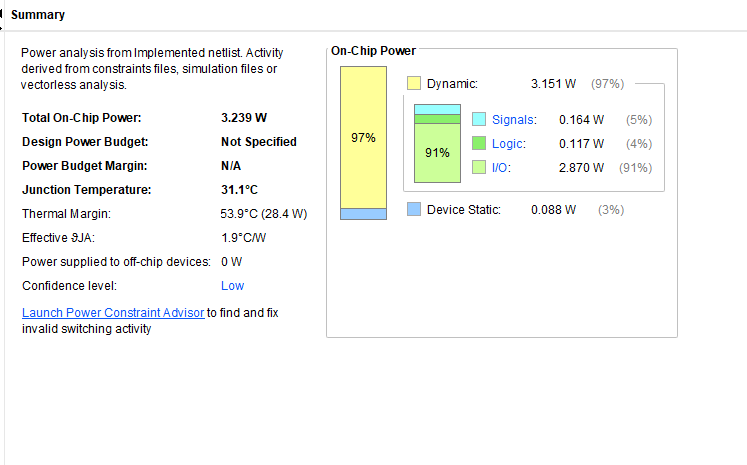
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

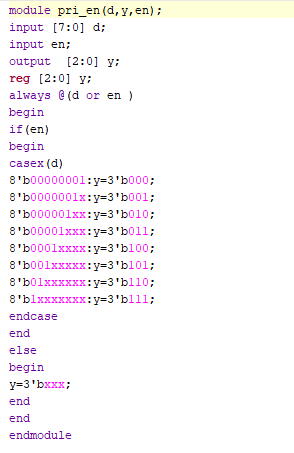


POWER REPORT:-

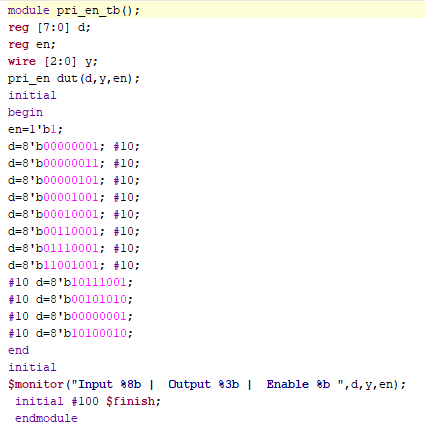


Q20. PRIORITY ENCODER

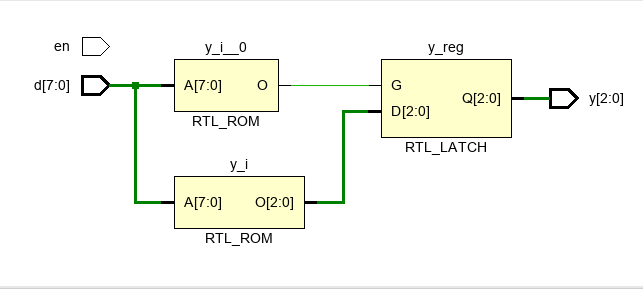
VERILOG CODE:-



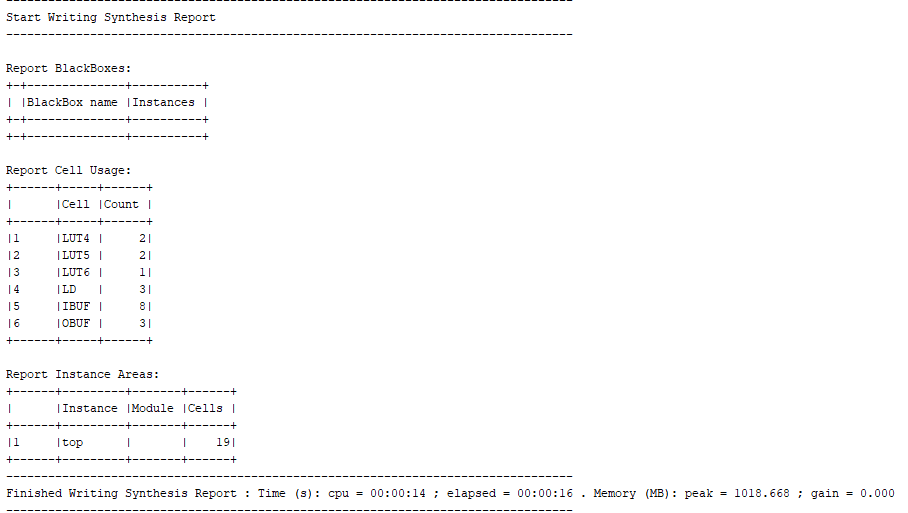
TEST BENCH:-



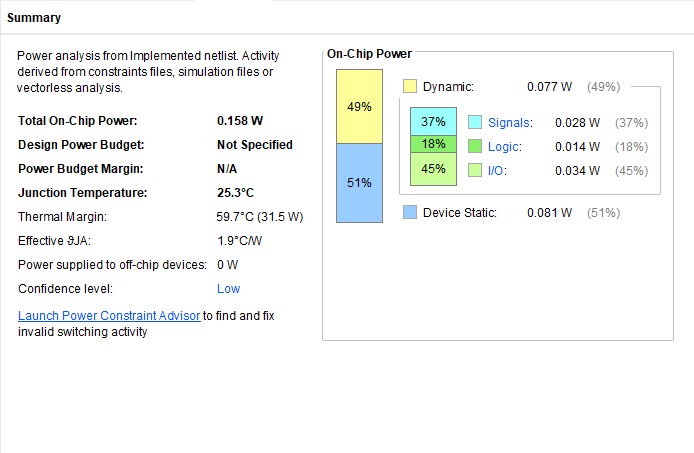
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

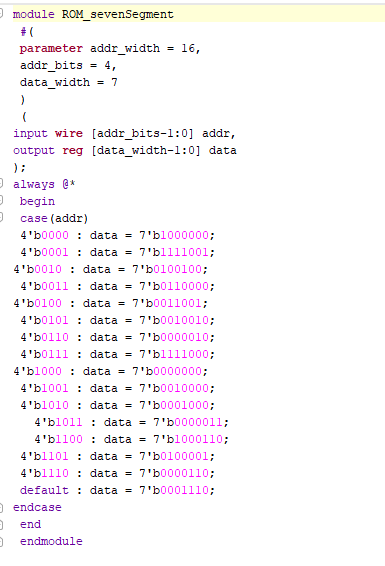


POWER REPORT:-

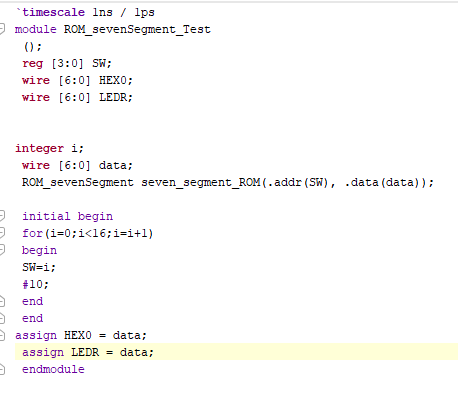


Q21. SEVEN SEGMENT DISPLAY USING ROM

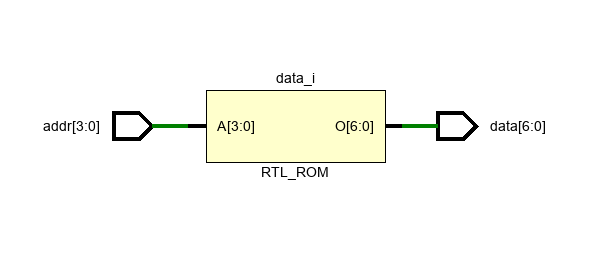
VERILOG CODE:-



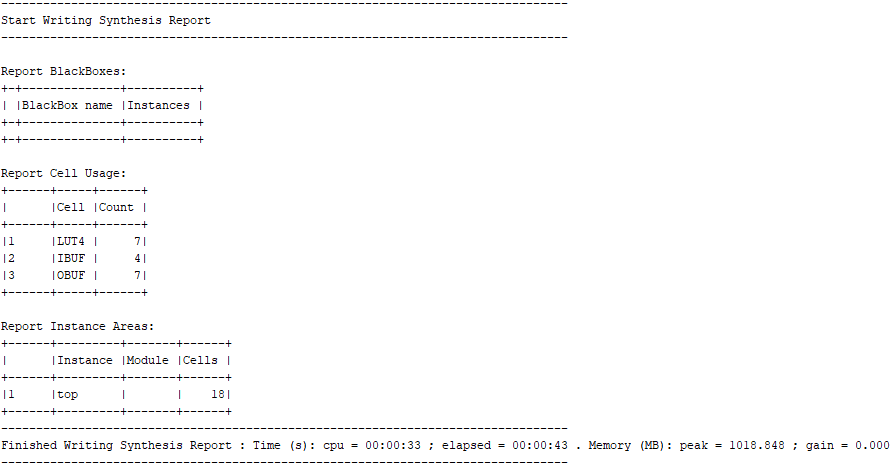
TESTBENCH:-



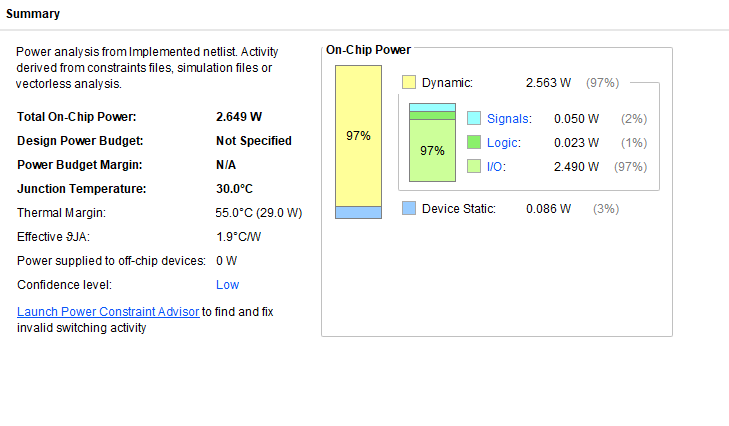
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

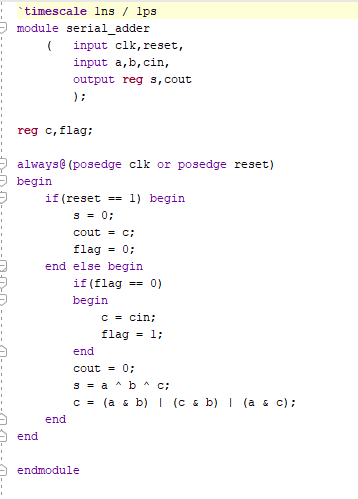


POWER REPORT:-

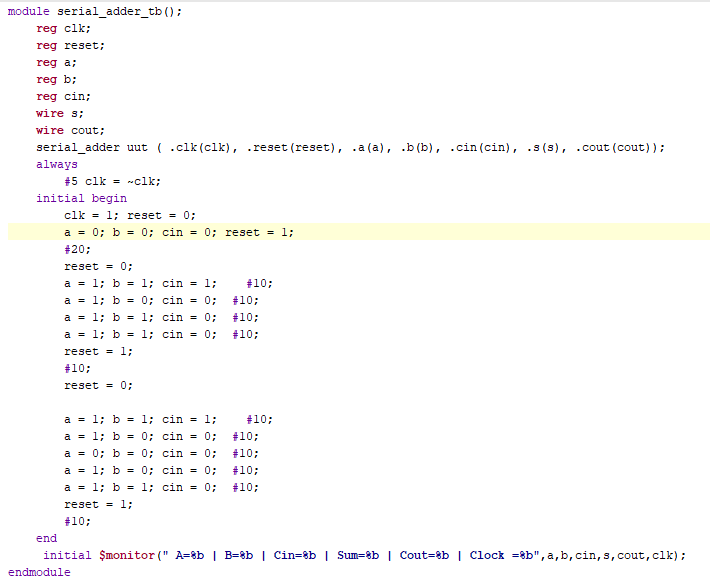


Q22. SERIAL ADDER

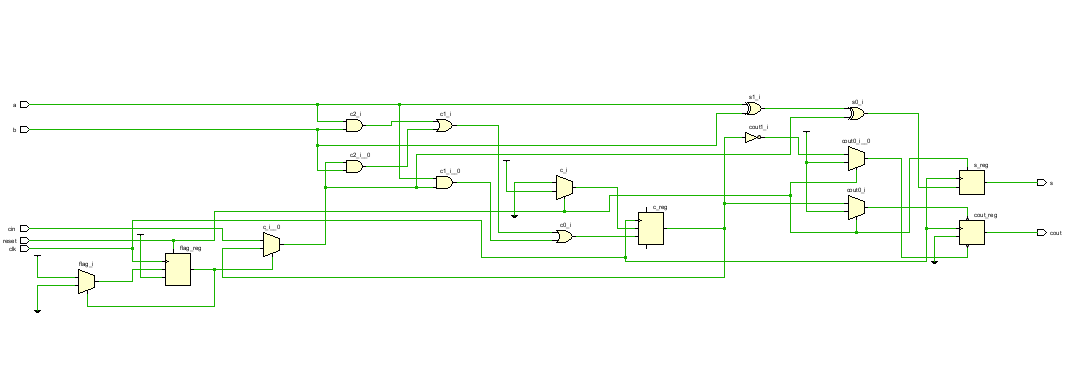
VERILOG CODE:-



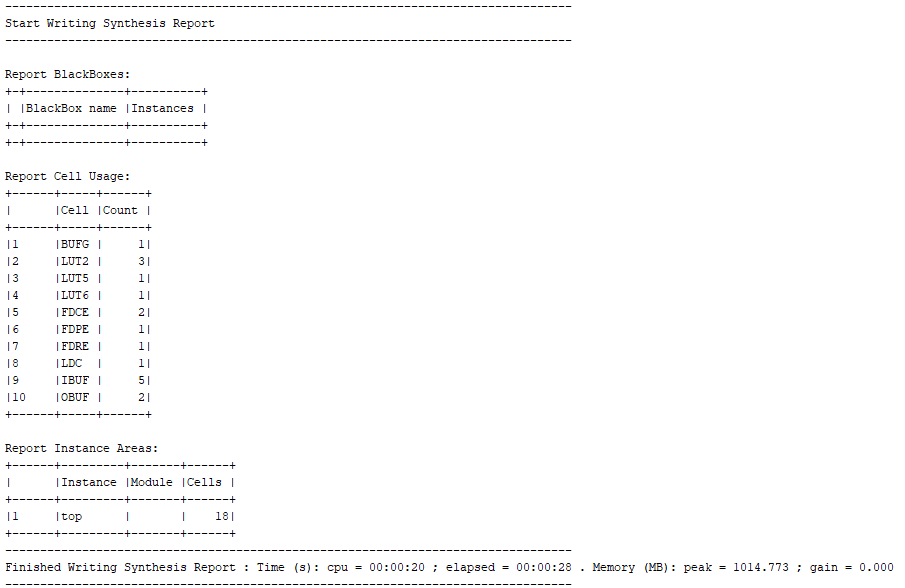
TESTBENCH:-



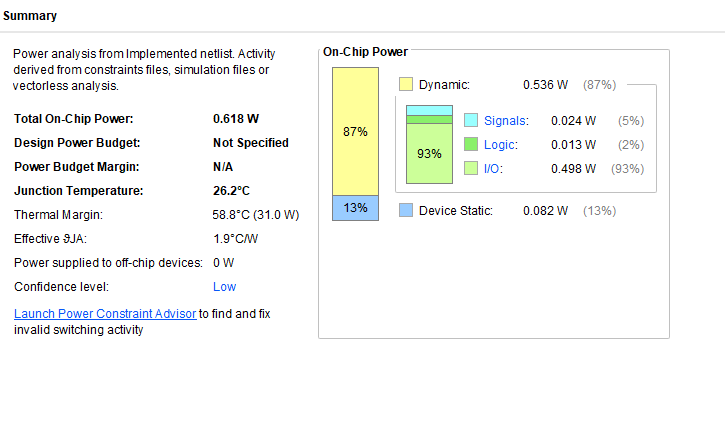
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

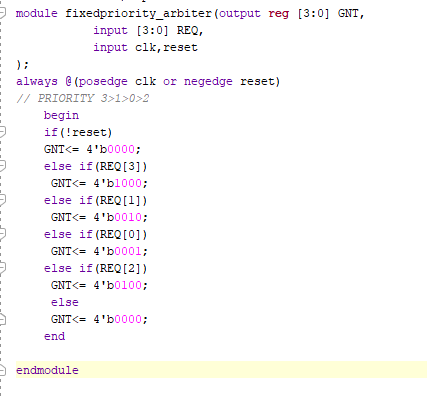


POWER REPORT:-

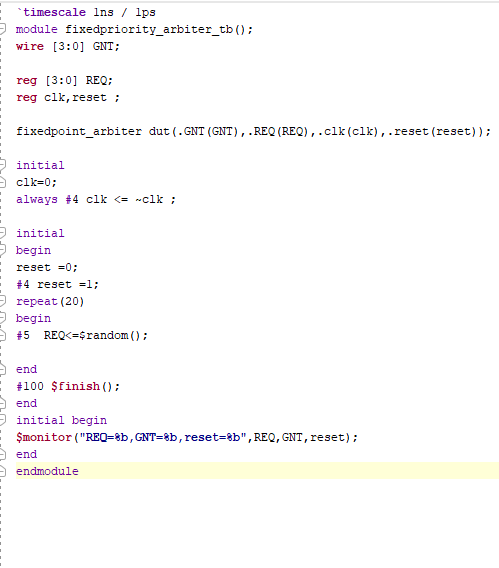


Q23. FIXED PRIORITY ARBITER

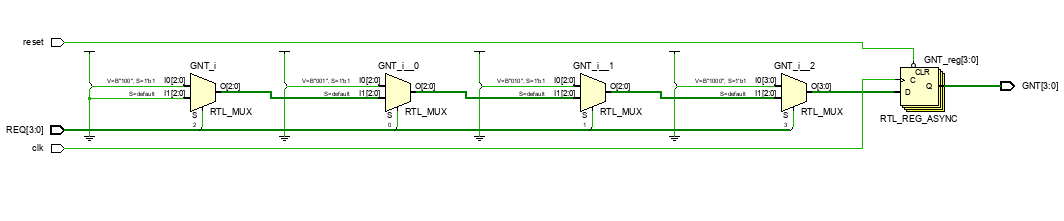
VERILOG CODE:-



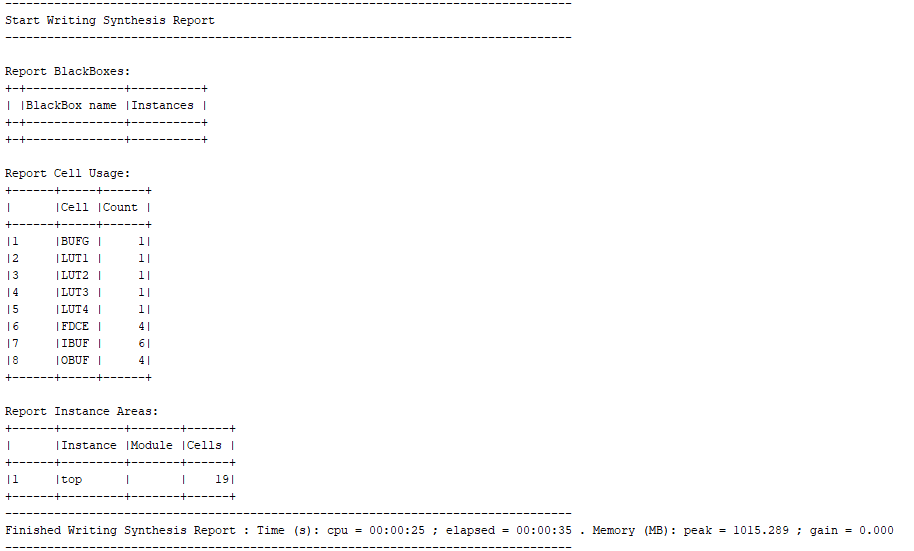
TESTBENCH:-



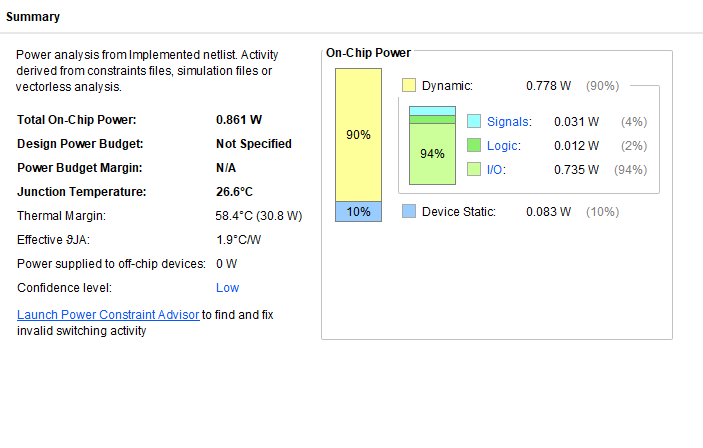
RTL SCHEMATIC:-



SYNTHESIS REPORT:-

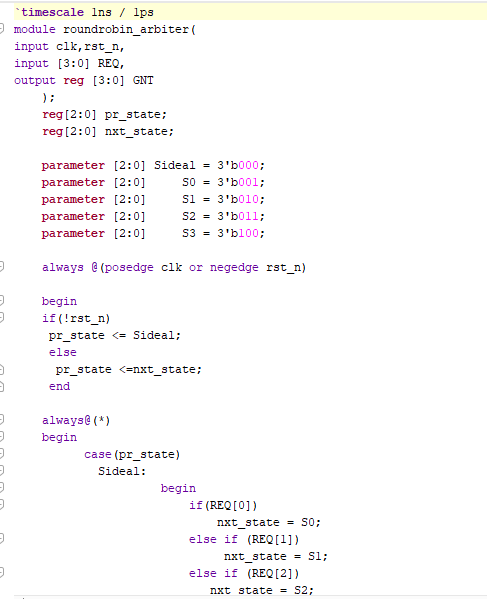


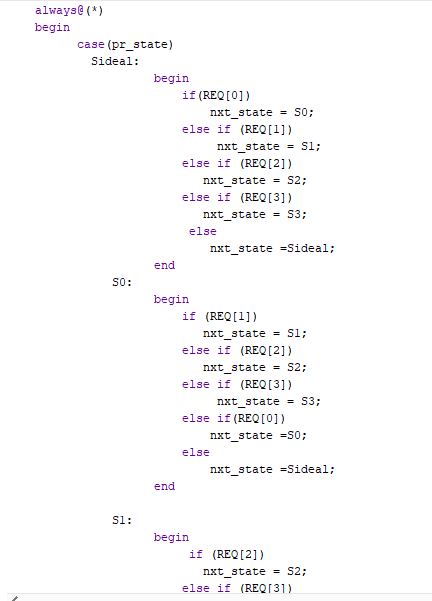
POWER REPORT:-

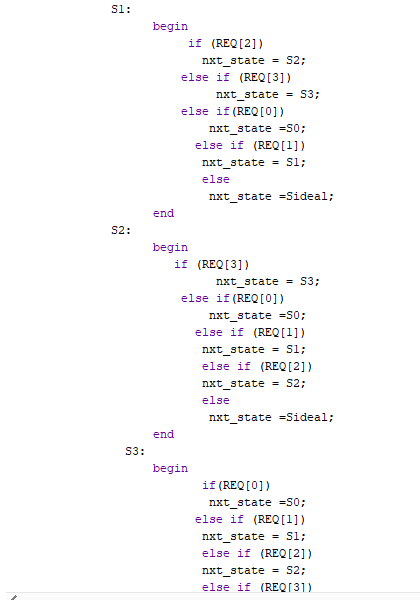


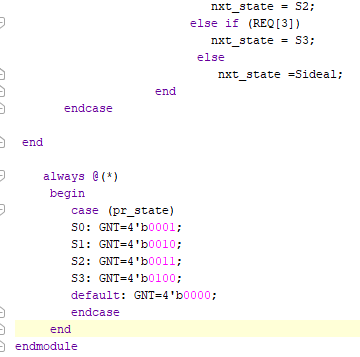
Q24. ROUND ROBIN ARBITER

VERILOG CODE:-

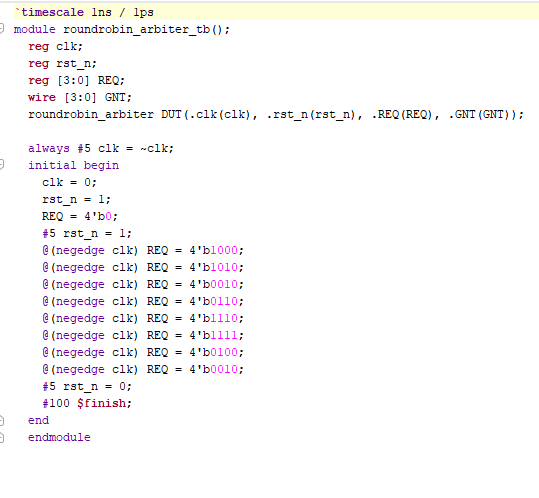




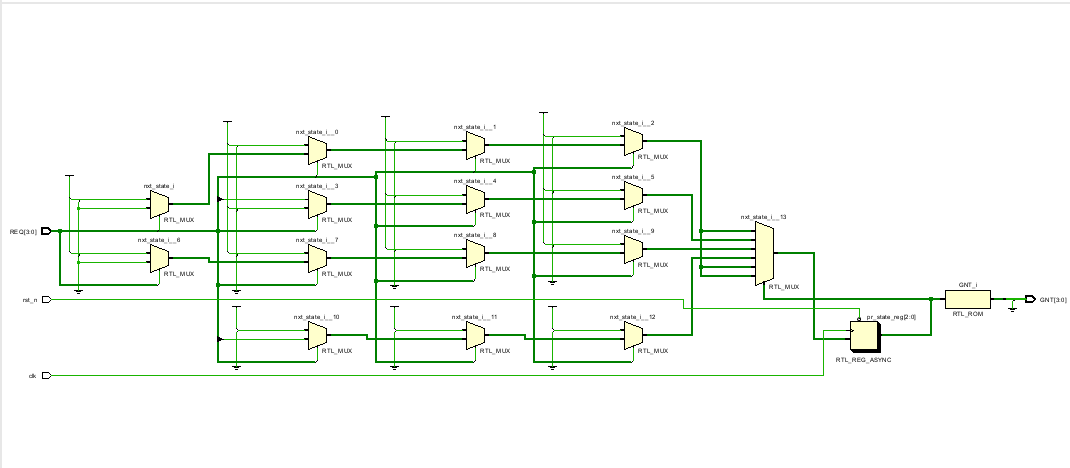




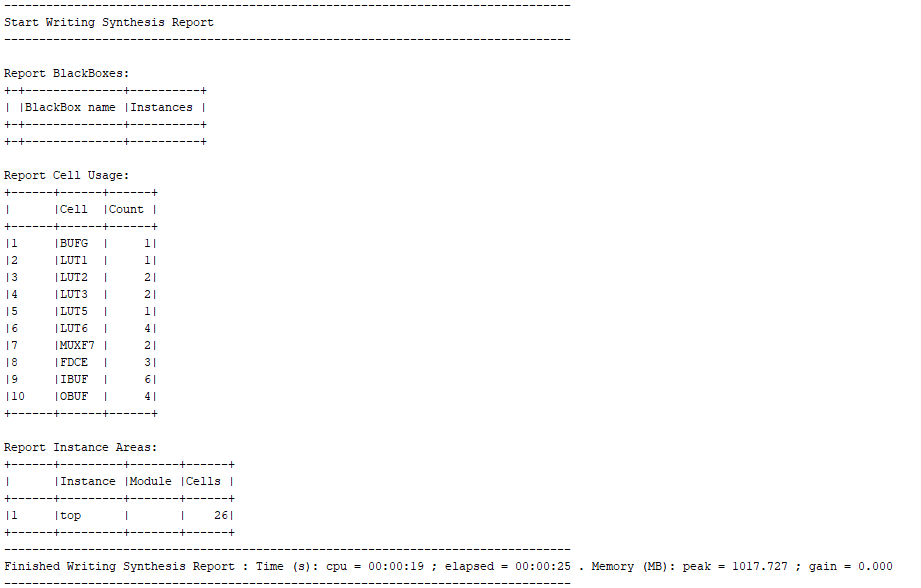
TESTBENCH:-



RTL SCHEMATIC:-



SYNTHESIS REPORT:-



POWER REPORT:-

